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Supplementary materials for

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1 Proof of Property 1

$w(t_i, s_k) = 1$ means that t_i is the output of s_k, and $w(t_j, s_k) = -1$ means that t_j is the input of s_k. Thus, it takes one step to conduct t_j after finishing the procedures of t_i, meaning $l_{ij} = 1$.

2 Proof of Property 2

If $l_{ik} > 0$, there exists a path in E as $\left\{(t_i, s_{i_1}), (s_{i_1}, t_{i_1}), (t_{i_1}, s_{i_2}), ..., (t_{i_{l_{ik}-1}}, s_{i_{l_{ik}}}), (s_{l_{ik}}, t_k)\right\}$. Similarly, when $l_{kj} > 0$, we have a path as $\left\{(t_k, s_{j_1}), (s_{j_1}, t_{j_1}), (t_{j_1}, s_{j_2}), ..., (t_{j_{l_{kj}-1}}, s_{l_{kj}}), (s_{j_{l_{kj}}}, t_j)\right\}$. Hence, there has a path from t_i to t_j as $\left\{(t_i, s_{i_1}), (t_{i_1}, s_{i_2}), \cdots, (t_{i_{l_{ik}-1}}, s_{i_{l_{ik}}}), \cdots, (t_{j_{l_{kj}-1}}, s_{l_{kj}}), (s_{j_{l_{kj}}}, t_j)\right\}$ with the total number of steps as $l_{ik} + l_{kj}$, so $l_{ij} = l_{ik} + l_{kj}$.

3 Proof of Property 3

$l_{ij} > 0$ means that t_i is l_{ij} steps behind t_j. Thus, it takes l_{ij} steps to conduct t_j after finishing the procedures of t_i. Hence, $l_{ji} = -l_{ij}$.

4 Proof of Property 4

If t_i is directly linked to the system inputs, there is no need to add any other test point to obtain the measurement of t_i. Hence, $c(t_i) = \Delta c(t_i)$.

5 Proof of Property 5

To obtain the measurement results of t_i, the test point set $\{t_j | l_{ij} = 1\}$ needs to be validated. Hence, to obtain the test set prepared, the minimum test cost is $\max(c(t_j) | l_{ij} = 1)$.

Thus, the test cost to add t_i into the test strategy is $\Delta c(t_i) + \max(c(t_j) | l_{ij} = 1)$.

6 Proof of Property 6

If t_k is assigned to the test strategy, the measurement of t_k is already obtained during the diagnosis procedures. Hence, the cost to re-use measurement from t_k is 0.

7 Proof of Property 7

As Property 5, the preparation cost to measure t_i is $\max\left(c\left(t_i\right)|l_{ij}=1\right)$. Since $\max\left(c\left(t_i\right)|l_{ij}=1\right) = c\left(t_k\right)$, we have $\hat{c}\left(t_i|t_k\right) = c\left(t_i|t_k\right)$. Also, if $\hat{c}\left(t_i|t_k\right) = c\left(t_i|t_k\right)$, according to Eq. (6), we have $c\left(t_k\right) = \max\left(c\left(t_i\right)|l_{ij}=1\right)$.

8 Proof of Property 8

If $l_{ik}=0$, then t_i and t_k are independent with each other, and the conditional process cost of t_i equals $c\left(t_i\right)$.

9 Proof of Property 9

If t_k is assigned to the test strategy, then t_k and the test points ahead of t_k are all added into the selected test set. According to Property 6, we have $c\left(t_k\right)=0$. From Property 6, the original cost to add test point t_i into the test strategy is $c\left(t_i\right)=\Delta c\left(t_i\right)+\max\left(c\left(t_j\right)|l_{ij}=1\right)$. Thus, $c\left(t_i\right)$ depends on the related test point t_j with the maximum process cost. If t_j has no relationship with t_k, then the conditional cost of t_j as $c\left(t_j|t_k\right)$ equals $c\left(t_j\right)$. Hence, Eq. (8) holds. If t_j has the relationship with t_k, then the cost to conduct previous test for t_j turns to 0. Hence, the process cost turns to $c\left(t_j|t_k\right)$, and Eq. (8) holds.

10 Proof of Property 10

If $\max\left(c(t_j|t_{k_1},t_{k_2},\cdots,t_{k_{m-1}})|l_{ij}=1\right)$ is $c\left(t_{k_m}|t_{k_1},t_{k_2},\cdots,t_{k_{m-1}}\right)$, according to Property 9, Eq. (9) holds.

11 Proof of Property 11

If $l_{ik_m}<0$, t_i is l_{ik_m} steps ahead of t_{k_m}. Hence, the measurement of t_{k_m} has no influence on measuring t_i. Therefore, we have $c\left(t_i|t_m\right)=c\left(t_i|t_{k_{m-1}}\right)$.

12 Proof of Property 12

If $\tilde{T}$ is added into the test strategy, we have $c\left(t_{k_p}|\tilde{T}\right)=0$, where t_{k_p} is the pth assigned test point of the kth AND node of the test strategy. Hence, we have $\max\left(c\left(t_j|\tilde{T}\right)|l_{ij}=1\right)=\max\left(c\left(t_j|t_{k_1},t_{k_2},\cdots,t_{k_{m-1}}\right)\right)$, and Eq. (10) holds.

13 Details of the real-world applications

The intermediate frequency (IF) signal conditioning circuit is presented in Fig. S1. The system structure depicted in Fig. S2 includes lowpass filters (LPFs), preamplifiers, balun filters, bandpass filters (BPFs), program-controlled circuits, anti-alias filters, and analog-to-digital converters (ADCs).

Based on engineering experience, 13 fault locations are considered, and 15 potential test points are provided during diagnosis. The locations of the fault states and tests are presented in Fig. S3. The 13 fault locations represent different fault states of 8099 amplifier (AMP), Blum, BPF, variable gain amplifier (VGA), and LPF in the target system. s_1 and s_2 represent the failure of feedback resistance and the failure of compensation capacitor of 8099 AMP, respectively. s_3 and s_4 are the open circuit of filter resistance and the open circuit of filter capacitor of Blum, respectively. s_5 and s_6 are the failure of resistance tolerance and the failure of capacitor tolerance of BPF, respectively. s_7 is the short circuit of resistance of BPF. s_8 and s_9 are the open circuit of coupling capacitor and the short circuit of bypass capacitor of VGA, respectively. s_{10}

is the open circuit of feedback of VGA. s_{11} represents the reduction of coupling capacitor or bypass capacitor of VGA. s_{12} and s_{13} are the failure of resistance tolerance and the failure of capacitor tolerance of LPF, respectively.

Each test point has the same cost consumption. The dependence information is presented in Table S1. Considering the influence of each fault state, the dependence matrix is built based on the relationship between the failure modes and the test procedures. For example, the failure of compensation capacitor (s_2) can cause abnormal observation of $V_{2\mathrm{pp}}(t_2)$. Since the abnormality of $V_{2\mathrm{pp}}(t_2)$ can influence other electric characteristics of different parts of the target system, the abnormality can also be detected on $V_{3\mathrm{pp}}(t_4)$, $V_{3\mathrm{dc}}(t_5)$, $V_{4\mathrm{pp}}(t_8)$, $V_{4\mathrm{dc}}(t_9)$, $V_{5\mathrm{ms}}(t_{14})$, $f_5(t_{15})$, and $V_{6\mathrm{pp}}(t_{16})$, sending the information of signal-to-noise ratio (SNR) decreasing. Since $\{s_5, s_6\}$ and $\{s_{10}, s_{12}\}$ share the same information, the system contains two fuzzy sets with all test points.

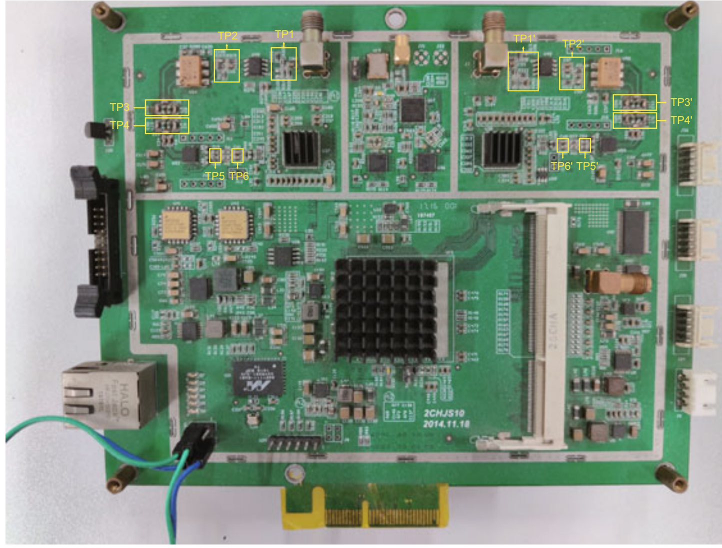

Fig. S1 System board of the real-world applications

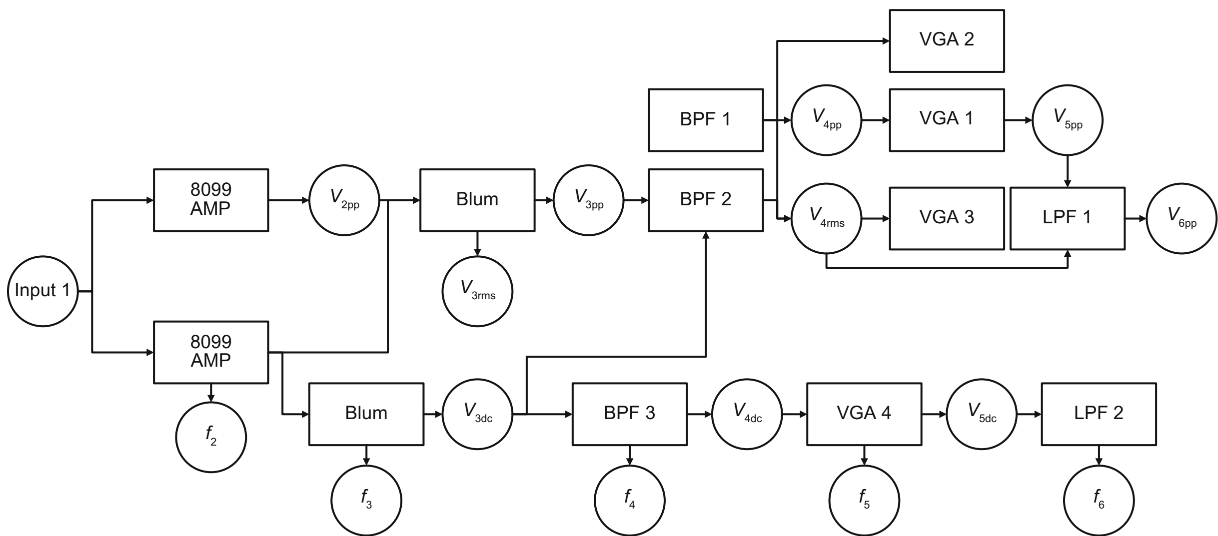

Fig. S2 System structure of the real-world applications

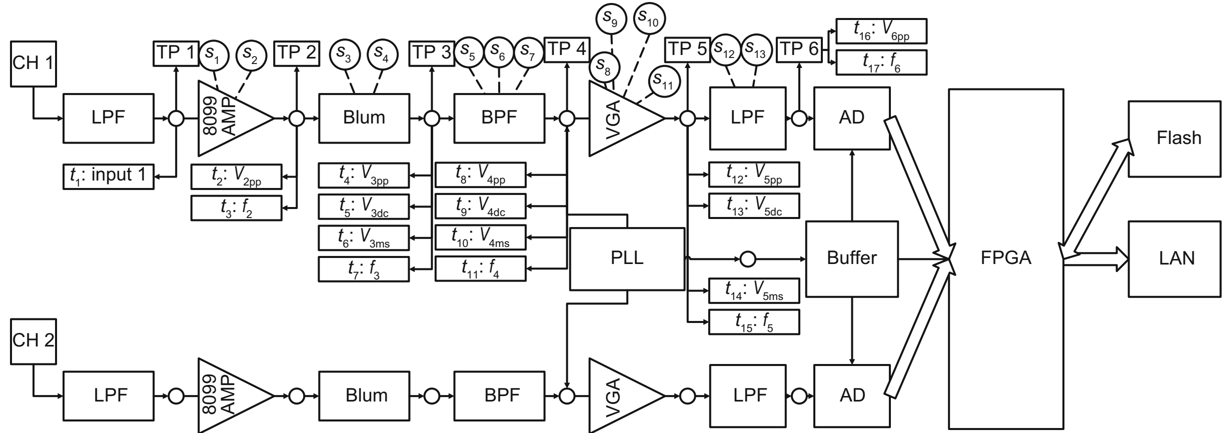

Fig. S3 Signal topology of the real-world applications (FPGA: field programmable gate array; AD: analog digital; TP: test point; PLL: phase locked loop; CH: channel)

Table S1 Dependence matrix of the real-world cases

Fault state	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}	t_{16}	t_{17}	$p(s_i)$
s_1	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1	1	0	0.1
s_2	0	0	1	0	1	0	0	1	1	0	0	0	0	1	1	1	0	0.1
s_3	0	0	0	1	1	0	0	1	1	0	0	0	0	1	1	1	0	0.1
s_4	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	0.1
s_5	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0.1
s_6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0.1
s_7	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	0.1
s_8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0.1
s_9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0.1
s_{10}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0.1
s_{11}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0.1
s_{12}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0.1
s_{13}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0.1
Dependent cost	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Test process cost	0	1	1	2	1	1	1	2	2	2	2	3	3	2	3	3	4	