



## A wideband frequency-shift keying demodulator for wireless neural stimulation microsystems\*

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**Abstract:** This paper presents a wideband frequency-shift keying (FSK) demodulator suitable for a digital data transmission chain of wireless neural stimulation microsystems such as cochlear implants and retinal prostheses. The demodulator circuit derives a constant frequency clock directly from an FSK carrier, and uses this clock to sample the data bits. The circuit occupies 0.03 mm<sup>2</sup> using a 0.6 μm, 2M/2P, standard CMOS process, and consumes 0.25 mW at 5 V. This circuit was experimentally tested at transmission speed of up to 2.5 Mbps while receiving a 5~10 MHz FSK carrier signal in a cochlear implant system.

**Key words:** Biomedical implants, CMOS, Demodulator, Frequency-shift keying (FSK), Cochlear implant

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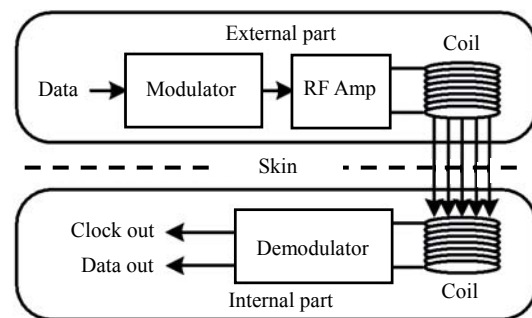
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### INTRODUCTION

Cochlear implants have been very successful in restoring auditory function in individuals who suffer from sensorineural deafness (Rauschecker and Shannon, 2002). A generic cochlear implant usually consists of an external part and an internal part, which are connected by an inductive transcutaneous link, as illustrated in Fig.1. The link sends both data and power to an internal circuit. The output data from a speech processor are modulated and amplified successively so that it can be transmitted through the skin to inside the human body. The demodulator of the internal part deals with the carrier and recovers the received serial data stream as well as a constant frequency clock from which to sample the data bits.

In contrast, visual prostheses have not yet been widely utilized in the blind though extensive research has been performed (Zrenner, 2002). One of the major



**Fig.1 Digital data transmission chain of a cochlear implant**

technological challenges of an implantable vision restoration device is to achieve a wide bandwidth with a carrier frequency that is limited to about 20 MHz. This is due to the high tissue electromagnetic absorption at higher frequencies (Lin, 1986) as well as the coupled coils self-resonance. Although power-transmission efficiency and coupling insensitivity have been comprehensively discussed (Ko *et al.*, 1977; Heetderks, 1988; Zierhofer and Hochmair, 1990; 1996; Galbraith *et al.*, 1987), there are few

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studies that focus on the aspect of bandwidth of this inductive transcutaneous link (Ghovanloo, 2004). So far, amplitude shift keying (ASK) has been commonly used in the above applications because of its simple modulation and demodulation circuitry (Mcdermott, 1989; Zierhofer *et al.*, 1995; Liu *et al.*, 2000; Suaning and Lovell, 2001; Troyk, 2001). Unfortunately, this method cannot offer high-bandwidth data transmission because it needs high-order filters with sharp cutoff frequencies, whose large capacitor is difficult to be integrated (Ghovanloo, 2004). Even though remedies such as suspended carrier modulation (Zierhofer *et al.*, 1995; Troyk, 2001) can be utilized to avoid these high-order filters by turning the carrier on and off to boost the modulation index by up to 100%, data rates above 1 Mbps have not been reported.

To tackle the bandwidth challenge described above, a wideband frequency-shift keying (FSK) protocol has been proposed, in which  $f_0$  is twice  $f_1$  (Ghovanloo, 2004). In this protocol, logic “1” is transmitted by a single cycle of the carrier  $f_1$ , and logic “0” is transmitted by two cycles of the carrier  $f_0$ , as shown in Fig.2. Several demodulators, which are based on measuring the period of each received carrier cycle, have been designed for this protocol (Ghovanloo, 2004).

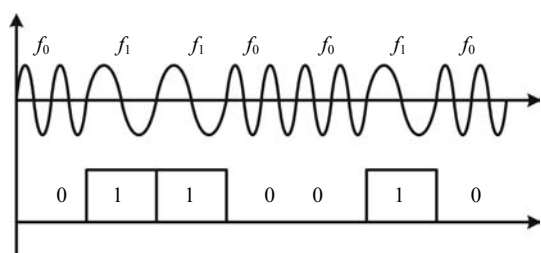


Fig.2 FSK data transfer protocol

In this paper, a new FSK demodulator for this protocol is presented. The demodulator used in this work significantly increases the data transmission bandwidth for wirelessly operating a cochlear implant system.

METHODS

Trace 1 and Trace 2 of Fig.3a depict an example

of a bit pattern and the FSK carrier sequence associated with it respectively. The FSK carrier signal is treated as a sinusoidal signal and squared up by a clock regenerator (Ghovanloo, 2004). The output signal CKin (Trace 3 of Fig.3a) contains critical timing information, from which a constant-frequency clock can be derived. Clock recovery from a Manchester coding bit stream can be fulfilled using a monoflop (Zierhofer and Hochmair, 1996). The same method can be utilized in this application, as shown in Fig.3b. Clock recovery from CKin is accomplished by a monoflop, which will generate a negative pulse of length  $Td$  every time it is triggered by a positive transition of its input (CKin) during quiescent state, i.e., its output (Clock-out) is high. Trace 4 of Fig.3a shows the output signal of the monoflop, which serves as basic clock signal for further processing of the data stream. Trace 5 of Fig.3a depicts the demodulated data signal, which is acquired by sampling CKin at each falling edge of Clock-out. Theoretically, correct bit synchronization takes place if the monoflop time constant  $Td$  meets the following condition:

$$\frac{1}{f_0} < Td < \frac{3}{2f_0}, \tag{1}$$

where  $f_0$  is the frequency presenting bit ‘0’.

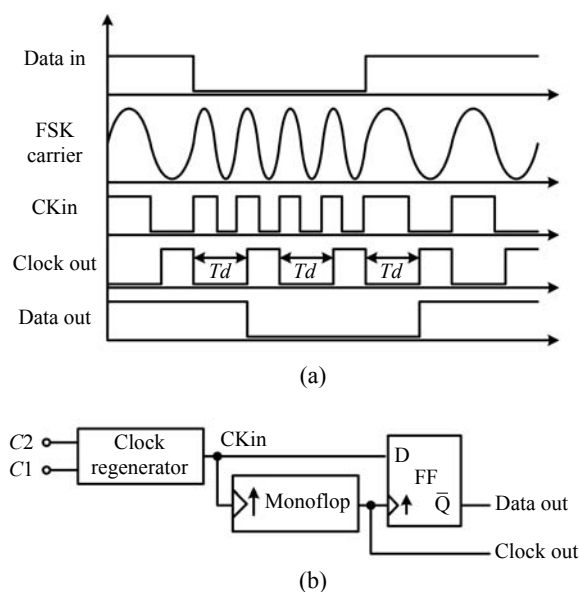


Fig.3 FSK demodulation methods. (a) Principle of demodulation; (b) Block diagram of the demodulator

Fig.4 shows the block diagram of the monoflop, in which a delay element capable of postponing the rising edge of its input signal for a period of  $Td$  is used to control the duration of the output pulse. In the quiescent state (Clock-out is high), the two inputs of the NAND are reverse because of the inverter, i.e., one of the two inputs is low. As a result, the output of the NAND (Clock-out) is high which makes the latch ready to sample CKin. When CKin is low, Node B is low and Node A is high. A positive transaction of CKin drives Node B high while Node A remains high because the delay element defers the transition, so that Clock-out is set low. Therefore, the latch goes into hold state and ignores any variation of CKin. After a delay  $Td$ , the output of the delay element becomes high and Node A is pulled low, thus, Clock-out goes high again. A pulse of length  $Td$  is created.

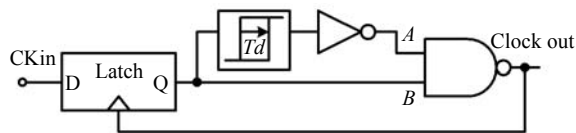


Fig.4 Block diagram of the monoflop

Fig.5 shows the schematic of the delay element (Zhang et al., 2005). The transistors  $M1$  and  $M2$  are connected as a current mirror. Thus the current in the transistor  $M2$  is constant as the reference current source  $I_{ref}$ , which is also required by stimulation circuit of the whole microsystem (Zierhofer et al., 1995; Liu et al., 2000; Suaning and Lovell, 2001). At the start of the rising edge of CKin, Node A discharges via capacitors  $C1$ ,  $C2$  and a constant current  $I_{ref}$ . When the voltage of Node A reaches the threshold

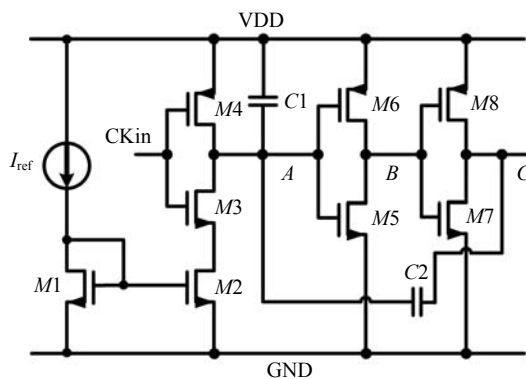


Fig.5 Schematic of the delay element

voltage of the subsequent inverter, the delay process is finished. The delay time can be roughly calculated by the following equation:

$$Td = \frac{(C1 + C2) \times V_{TH}}{I_{ref}}, \quad (2)$$

where  $V_{TH}$  is the threshold voltage of the inverter and  $I_{ref}$  is the drain current in the transistor  $M1$  or  $M2$ .

Fig.6 illustrates some simulation results of the demodulator. When bit stream "1100010011" is modulated as an FSK carrier and applied to the demodulator circuit, the FSK carrier is converted to similar square wave CKin. It is clearly shown that constant frequency clock signal Clock-out and serial data signal Data-out are generated. On every rising edge of Clock-out, Data-out can be read the same as the original binary data.

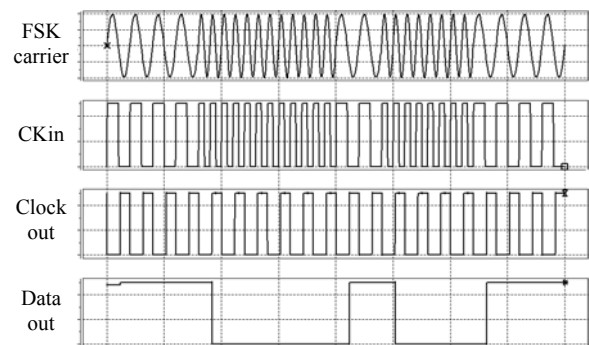


Fig.6 Simulated waveforms

The circuit is implemented instead of an ASK demodulator in a chip used for a cochlear implant system (Dong et al., 2004), which is as shown in Fig.7 and fabricated in  $0.6 \mu\text{m}$  2M/2P standard CMOS process. Fig.8 shows the block diagram of the chip. Power and data are received from a coil on the platform. The carrier is rectified and regulated to generate 5 V power supply for the chip to work. The FSK demodulator receives the modulated carrier and recovers data and clock signals. The control logic unit decodes these data and obtains the parameters of each stimulus such as intensity, position and duration, and sends these parameters to DAC and switch array respectively. The DAC generates stimulus current of different amplitude according to the intensity pa-

parameter, while the position and duration of the current is decided by the switch matrix. A voltage monitor compares the power supply with a reference voltage regularly and sends a warning signal to reset the whole system when the power voltage is below normal level. A bandgap circuit is used to provide reference current for demodulator and DAC. A back telemetry unit is also included to make it possible to send out some useful information such as the power supply voltage and resistance between electrodes.

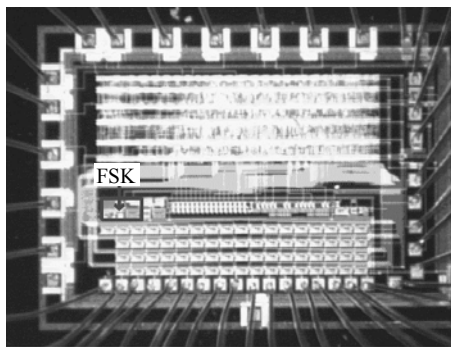


Fig.7 Die microphotograph

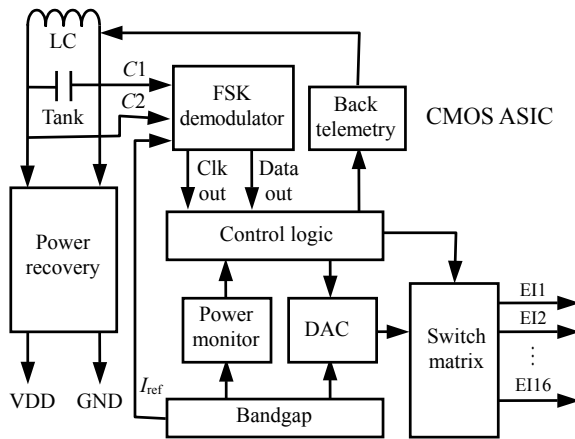


Fig.8 Block diagram of a chip for cochlear implant

EXPERIMENTAL RESULTS

The demodulator circuit has been tested separately and Fig.9 shows the measured waveforms, with  $f_0$  and  $f_1$  set to 10 MHz and 5 MHz respectively. With a 5 V supply the delay element of the monoflop generates a period of 112 ns which is inside the desired

range (100~150 ns). All of the traces are labelled according to their names in the simulation and circuit diagrams.

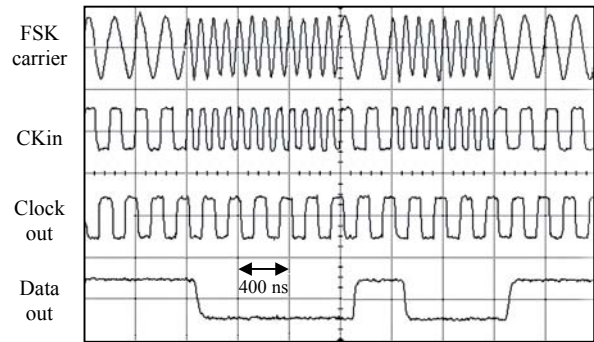


Fig.9 Measured waveforms

It can be seen that the FSK demodulator circuit is functioning as expected from the simulations, up to 2.5 Mbps, which guarantees the whole chip for cochlear implant to work correctly. Table 1 summarizes some of the performance specifications of the demodulator circuit.

Table 1 Specifications of the demodulator circuit


Parameter	Value
Process technology	0.6 $\mu\text{m}$ 2M/2P Std-CMOS
Circuit area	0.03 $\text{mm}^2$
Carrier frequency	5/10 MHz
Max data rate	2.5 Mbps
Supply voltage	5 V
Power dissipation	0.25 mW

CONCLUSION

A wideband FSK demodulator dedicated to a digital data transmission chain of wireless neural stimulation microsystems is presented. The demodulator circuit converts the FSK carrier signal to digital signal directly, from which it derives a constant frequency clock, and uses this clock to sample the data bits. The circuit is fabricated in a 0.6  $\mu\text{m}$ , 2M/2P, standard CMOS process, and occupies 0.03  $\text{mm}^2$ . This circuit was experimentally tested up to 2.5 Mbps while receiving a 5~10 MHz FSK carrier signal in a cochlear implant system. The power consumption is 0.25 mW at 5 V.

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