Journal of Zhejiang University-SCIENCE C (Computers & Electronics)
ISSN 1869-1951 (Print); ISSN 1869-196X (Online)
www.zju.edu.cn/jzus; www.springerlink.com
E-mail: jzus@zju.edu.cn

New Technique:

A low drift current reference based on PMOS temperature correction technology

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Received Apr. 15, 2012; Revision accepted Aug. 15, 2012; Crosschecked Oct. 22, 2012

Abstract: A low drift current reference based on PMOS temperature correction technology is proposed. To achieve the minimum temperature coefficient (TC), the PMOS cascode current mirror is designed as a cross structure. By exchanging the bias for two layers of the self-biased PMOS cascode structure, the upper PMOS, which is used to adjust the TC together with the resistor of the self-biased PMOS cascode structure, is forced to work in the linear region. As the proposed current reference is the on-chip current reference of a high voltage LED driver with high accuracy, it was designed using a CSMC 1 μm 40 V BCD process. Simulation shows that the TC of the reference current was only 23.8×10^{-6}/°C over the temperature range of −40–120 °C under the typical condition.

Key words: Current reference, Cross structure, PMOS cascode, Temperature coefficient, Low drift
doi:10.1631/jzus.C1200112 **Document code:** A **CLC number:** TN432

1 Introduction

Current reference is used in almost every analog and mixed-signal chip, to establish the quiescent condition or provide a reference current for other modules integrated in chip, such as regulators, amplifiers, comparators, and oscillators. High precision current reference is required in many chips because the accuracy of the current reference affects directly the precision of the chip and even the system.

Different circuit structures have been proposed to produce a precision current reference insensitive to temperature, supply voltage, and process parameters. Most of them focus on minimizing their temperature dependence. Traditional methods for temperature compensation rely on specific device parameter values for proper performance. A zero temperature coefficient (TC) is difficult to obtain since the TCs of the devices are not linear and difficult to predict. Moreover, the device parameters vary randomly with the process and working conditions. The current reference can be adjusted only in a typical condition and the TC of the current is obtained only for a single, non-arbitrary value.

There have been many circuit structures and temperature compensation methods. Some current references using a variation of the bandgap voltage reference circuit have been proposed (Khan *et al*., 2003; Yang *et al*., 2009; Chun and Lehmann, 2010). These circuit structures take advantage of the opposite TC of V_{BE} and ΔV_{BE} of bipolar transistors, but the circuit design is relatively complex and needs more area cost due to the use of bipolar transistors. For example, an accurate current reference using temperature and process compensation current mirror was proposed by Yang *et al*. (2009). The method for temperature compensation in the proposed current reference is summing a proportional-to-absolute-temperature (PTAT) current and a complementary-to-absolute-temperature (CTAT) current, where the PTAT and CTAT currents are obtained from ΔV_{BE} and V_{BE}, respectively. Therefore, the design circuit of the

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proposed method is complex, with one generator of PTAT current, one generator of CTAT current, and one summing circuit to sum the two currents with opposite TC. Each circuit consists of many devices and consumes power. As it is hard to obtain exactly opposite PTAT and CTAT currents in all conditions, the summing generally cannot lead to a zero TC. The simulation result of this method is 228×10^{-6}/°C over a temperature range of −20–120 °C. Some other circuit structures have been proposed, exploiting the temperature dependence of the parameters of MOSFET transistors and resistors (Yoo and Park, 2007; Serrano and Hasler, 2008; Babu *et al.*, 2010; Osaki *et al.*, 2010; Yang *et al.*, 2011). These circuit structures are designed without bipolar transistors and cost less area. Yoo and Park (2007) proposed a self-biased CMOS current reference with compensation by simply subtracting two current outputs with the same dependence on supply voltage and temperature. For temperature compensation, they subtracted two positive TC currents, depending on the negative TC of the carrier mobility of MOSEFTs and resistors. Due to the difficulty in obtaining exactly the same temperature compensation for the two currents, and the reliance on process parameters, the TC of the current reference can be compensated in only one situation and is hard to minimize in different conditions. The simulation result of the TC of the current reference proposed by Yoo and Park (2007) is 60×10^{-6}/°C and the measurement result is 720×10^{-6}/°C over a temperature range of 0–120 °C. Serrano and Hasler (2008) proposed a method for temperature compensation using the TC of MOSEFTs and resistors. The proposed circuit achieves first-order temperature compensation by canceling the negative TC of an on-chip poly resistor with the positive TC of a MOSFET operating in the linear region. Experimental results showed that the TC of the proposed current reference is less than 130×10^{-6}/°C.

A novel circuit structure of low drift current reference is proposed in this paper. A cross structure created by exchanging the bias of two layers of the self-biased PMOS cascode structure current mirror is used, which makes the upper layer of PMOS work in the linear region to adjust the TC together with the resistor in the self-biased PMOS cascode structure. The proposed current reference obtains a low TC with a very simple circuit structure.

2 Circuit structure of the proposed low drift current reference

Fig. 1 shows the circuit structure of the low drift current reference proposed in this paper, which contains three parts: the start-up circuit, the PTAT current generating circuit, and the temperature correction circuit.

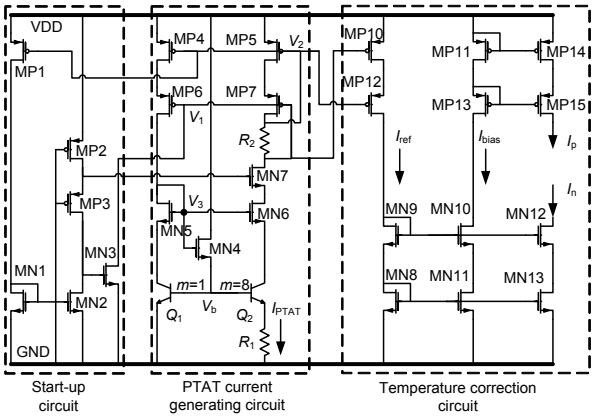

Fig. 1 Circuit structure of the proposed low drift current reference

The start-up circuit starts to work at the power-on time and pushes the circuit off the steady state. When VDD powers on, MP2 and MP3 begin to open, at the rising voltage of VDD. When the gate voltage of MN3 is approximately equal to VDD, MN3 opens, which pulls down V_1. Then, due to R_2, V_2 falls down with V_1, which makes MP4–MP7 open. As a result, V_3 uplifts to open MN4, and V_b also uplifts. After V_b is biased by MN4, Q_1 and Q_2 start to work. The circuit start-up is thus completed. As V_2 is low and MP1 is open, the current flowing through MN1 is copied to MN2 by MN1, the gate voltage of MN3 is pulled down, and NM3 is shut down. Therefore, the start-up circuit does not affect the operation of the other circuits. In the start-up circuit, MP1, MP2, and MP3 are designed to have large length and small width. The width/length ratio of switch MN2 is large, so the equivalent resistance is much less than those of MP2 and MP3. Therefore, the gate voltage of MN7 is dependent on those of MP2 and MP3.

The PTAT current generating circuit is designed to produce the PTAT current I_{PTAT}. Four P-type MOSFETs with the same width/length ratio, MP4–MP7, form a self-biased PMOS cascode structure

current mirror with a resistor R_2, forcing the currents flowing through Q_1 (I_1) and Q_2 (I_2) to be equal. Q_1 and Q_2 are bipolar transistors biased by MN4, and their collector current can be expressed as (Behzad, 2005)

$$I_{\mathrm{C}} = I_{\mathrm{S}} \exp(V_{\mathrm{BE}} / V_T),\ \ V_T = kT / q\ . \tag{1}$$

I_{S}, the saturation current, can be expressed as (Behzad, 2005)

$$I_{\mathrm{S}} \propto \mu k T n_i^{\,2}\ , \tag{2}$$

where

$$\mu \propto \mu_0 T^m,\ m \approx -3/2,$$
$$n_i^{\,2} \propto T^3 \exp[-E_{\mathrm{g}} / (kT)],\ E_{\mathrm{g}} \approx 1.12\ \mathrm{eV}.$$

Thus, we have

$$I_{\mathrm{S}} = bT^{4+m} \exp[-E_{\mathrm{g}} / (kT)]\,. \tag{3}$$

The TC of I_{S} is (Behzad, 2005)

$$\frac{\partial I_{\mathrm{S}}}{\partial T} = b(4+m)T^{3+m} \exp\left(\frac{-E_{\mathrm{g}}}{kT}\right) + \frac{E_{\mathrm{g}}}{kT} \exp\left(\frac{-E_{\mathrm{g}}}{kT^2}\right). \tag{4}$$

According to Eq. (1), V_{BE} is expressed as (Behzad, 2005)

$$V_{\mathrm{BE}} = V_T \ln(I_{\mathrm{C}} / I_{\mathrm{S}}). \tag{5}$$

The TC of V_{BE} is (Behzad, 2005)

$$\begin{aligned}\frac{\partial V_{\mathrm{BE}}}{\partial T} &= \frac{\partial V_T}{\partial T} \ln \frac{I_{\mathrm{C}}}{I_{\mathrm{S}}} - \frac{\partial I_{\mathrm{S}}}{\partial T} \frac{V_T}{I_{\mathrm{S}}} \\ &= \frac{V_T}{T} \ln \frac{I_{\mathrm{C}}}{I_{\mathrm{S}}} - (4+m)\frac{V_T}{T} - \frac{V_T E_{\mathrm{g}}}{kT^2} \\ &= \frac{1}{T}[V_{\mathrm{BE}} - (4+m)V_T - E_{\mathrm{g}} / q].\end{aligned} \tag{6}$$

When $V_{\mathrm{BE}} \approx 750$ mV,

$$\frac{\partial V_{\mathrm{BE}}}{\partial T} \approx -1.5\ \mathrm{mV/K},\ \ T = 300\ \mathrm{K}. \tag{7}$$

The TC of V_{BE} is negative.

In this design, the same model as qvn5 is chosen to implement Q_1 and Q_2, and the size ratio of Q_1 to Q_2 is 1:8, so $I_{\mathrm{S1}}=I_{\mathrm{S}}$, $I_{\mathrm{S2}}=8I_{\mathrm{S}}$. Due to the self-biased PMOS cascode structure current mirror, the currents flowing through Q_1 and Q_2 are the same, i.e., $I_1=I_2$. Ignoring the base current, ΔV_{BE} of Q_1 and Q_2 can be expressed as (Behzad, 2005)

$$\begin{aligned}\Delta V_{\mathrm{BE}} &= V_{\mathrm{BE1}} - V_{\mathrm{BE2}} = V_T \ln(I_1 / I_{\mathrm{S}}) - V_T \ln[I_2 / (8I_{\mathrm{S}})] \\ &= V_T \ln 8.\end{aligned} \tag{8}$$

The TC of ΔV_{BE} is (Behzad, 2005)

$$\frac{\partial(\Delta V_{\mathrm{BE}})}{\partial T} = \frac{k}{q} \ln 8,\ \ V_T = \frac{kT}{q}. \tag{9}$$

The voltage difference ΔV_{BE} of two bipolar transistors with different current densities is PTAT. In this structure, the bias voltage of Q_1 and Q_2 is $V_{\mathrm{b}}=V_{\mathrm{BE1}}=V_{\mathrm{BE2}}+I_{\mathrm{PTAT}}R_1$, where R_1 is the resistor made of the p-plus layer and its TC is positive. Then the current flowing through R_1 is also PTAT, expressed as

$$I_{\mathrm{PTAT}} = \frac{V_{\mathrm{BE1}} - V_{\mathrm{BE2}}}{R_1} = \frac{\Delta V_{\mathrm{BE}}}{R_1} = \frac{V_T \ln 8}{R_1}. \tag{10}$$

Since the TC of R_1 is positive and small enough, it can be expressed as

$$\frac{\partial I_{\mathrm{PTAT}}}{\partial T} = \frac{k \ln 8}{qR_1} - \frac{kT \ln 8}{qR_1^{\,2}} \frac{\partial R_1}{\partial T} \approx \frac{k \ln 8}{qR_1}. \tag{11}$$

The PTAT current I_{PTAT} is thus produced. In this circuit, MN5 and MN6 are used to make the currents of Q_1 (I_1) and Q_2 (I_2) equal. MN7 is used to obtain a same drain voltage as MN5 and MN6, to minimize the effect of channel modulation.

The temperature correction circuit adjusts the TC together with the resistor of the self-biased PMOS cascode structure in the PTAT current generating circuit using a cross structure. It is simplified as Fig. 2. MP5, MP7, and R_2 form a self-biased PMOS cascode structure. MP10 is biased by MP7 and MP12 is biased by MP5. In this condition, MP10 works in the linear region.

According to Fig. 2, we have

$$|V_{\mathrm{GS5}}| = |V_{\mathrm{GS12}}| + I_{\mathrm{ref}} R_{\mathrm{MP10}}\ . \tag{12}$$

Namely,

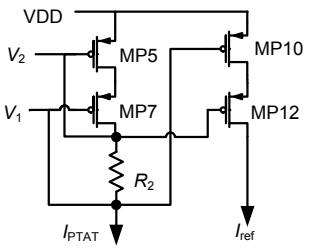

Fig. 2 The simplified diagram of the temperature correction circuit

$$\sqrt{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}=\sqrt{2I_{\mathrm{ref}}\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{12}}+I_{\mathrm{ref}}R_{\mathrm{MP10}}, \tag{13}$$

where R_{MP10} is the equivalent resistance of MP10 and can be expressed as

$$\begin{aligned}R_{\mathrm{MP10}}&=\frac{1}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{10}\,|V_{\mathrm{GS10}}-V_{\mathrm{TH}}|}\\&=\frac{1}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{10}(|V_{\mathrm{GS5}}-V_{\mathrm{TH}}|+I_{\mathrm{PTAT}}R_2)}\\&=\frac{1}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{10}\left(\sqrt{\dfrac{2I_{\mathrm{PTAT}}}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}+I_{\mathrm{PTAT}}R_2\right)}.\end{aligned} \tag{14}$$

The TC of R_{MP10} is

$$\begin{aligned}\frac{\partial R_{\mathrm{MP10}}}{\partial T}=&-\frac{1}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{10}\left(\sqrt{\dfrac{2I_{\mathrm{PTAT}}}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}+I_{\mathrm{PTAT}}R_2\right)^2}\\&\cdot\left\{I_{\mathrm{PTAT}}\frac{\partial R_2}{\partial T}+R_2\frac{\partial I_{\mathrm{PTAT}}}{\partial T}+\sqrt{\frac{1}{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}\frac{\partial I_{\mathrm{PTAT}}}{\partial T}\right.\\&\left.-\sqrt{\frac{I_{\mathrm{PTAT}}}{2\mu_{\mathrm{P}}{}^3C_{\mathrm{OX}}(W/L)_5}}\frac{\partial\mu_{\mathrm{P}}}{\partial T}\right\}.\end{aligned} \tag{15}$$

The target of the temperature correction circuit is to adjust the TC of the current I_{ref} to zero. Assuming the TC of I_{ref} is zero, we can obtain the TC from Eq. (13) as follows:

$$\begin{aligned}I_{\mathrm{ref}}\frac{\partial R_{\mathrm{MP10}}}{\partial T}=&\frac{\sqrt{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}{2\sqrt{I_{\mathrm{PTAT}}}}\frac{\partial I_{\mathrm{PTAT}}}{\partial T}\\&+\frac{\sqrt{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}C_{\mathrm{OX}}}\left(\sqrt{I_{\mathrm{PTAT}}(W/L)_5}-\sqrt{I_{\mathrm{ref}}(W/L)_{12}}\right)}{2\sqrt{\mu_{\mathrm{P}}}}\frac{\partial\mu_{\mathrm{P}}}{\partial T}.\end{aligned} \tag{16}$$

Because I_{PTAT} and the size of MP5 are restricted to the PTAT current generating circuit, and the other parameters are all process dependent, using k_1 and k_2 instead of the coefficients in Eq. (15), we have

$$\frac{\partial R_{\mathrm{MP10}}}{\partial T}=-\frac{1}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{10}}\left(k_1+k_2\frac{\partial R_2}{\partial T}\right), \tag{17}$$

where

$$\begin{aligned}k_1=&\frac{1}{\left(\sqrt{\dfrac{2I_{\mathrm{PTAT}}}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}+I_{\mathrm{PTAT}}R_2\right)^2}\\&\cdot\left\{\left(\sqrt{\frac{1}{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}+R_2\right)\frac{\partial I_{\mathrm{PTAT}}}{\partial T}\right.\\&\left.-\sqrt{\frac{1}{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}{}^3C_{\mathrm{OX}}(W/L)_5}}\frac{\partial\mu_{\mathrm{P}}}{\partial T}\right\},\\k_2=&\frac{I_{\mathrm{PTAT}}\dfrac{\partial R_2}{\partial T}}{\left(\sqrt{\dfrac{2I_{\mathrm{PTAT}}}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}+I_{\mathrm{PTAT}}R_2\right)^2}.\end{aligned}$$

Using k instead of the coefficient in Eq. (16), we have

$$I_{\mathrm{ref}}\frac{\partial R_{\mathrm{MP10}}}{\partial T}=k, \tag{18}$$

where

$$\begin{aligned}k=&\frac{\sqrt{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_5}}{2\sqrt{I_{\mathrm{PTAT}}}}\frac{\partial I_{\mathrm{PTAT}}}{\partial T}\\&+\frac{\sqrt{2I_{\mathrm{PTAT}}\mu_{\mathrm{P}}C_{\mathrm{OX}}}\left(\sqrt{I_{\mathrm{PTAT}}(W/L)_5}-\sqrt{I_{\mathrm{ref}}(W/L)_{12}}\right)}{2\sqrt{\mu_{\mathrm{P}}}}\frac{\partial\mu_{\mathrm{P}}}{\partial T}.\end{aligned}$$

According to Eqs. (17) and (18),

$$-\frac{k_1+k_2\dfrac{\partial R_2}{\partial T}}{\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{10}}=\frac{k}{I_{\mathrm{ref}}}. \tag{19}$$

Therefore,

$$I_{\mathrm{ref}}=-\frac{k\mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{10}}{k_1+k_2\dfrac{\partial R_2}{\partial T}}. \tag{20}$$

Here k is dependent only on $(W/L)_{10}$ because k_1 and k_2 are both positive constants. R_2 uses the resistor model rhm1k, which has a negative TC. Substituting Eqs.

(10) (I_{PTAT}), (14) (R_{MP10}), and (18) (I_{ref}) into Eq. (13), we can calculate the sizes of MP10 and MP12, $(W/L)_{10}$ and $(W/L)_{12}$, and a zero TC current I_{ref}.

The current I_{ref} is mirrored to obtain an output current I_{bias}, which provides current biases I_p and I_n for on-chip circuits.

The circuit structure of the proposed low drift current reference is a simple design. According to Eq. (8), it is not strict with the current, and any difference of the current just changes the coefficient of PTAT current, which can be adjusted by MP10 and R_2. The proposed method for temperature compensation is using the negative TC of resistor R_2, the positive TC of ΔV_{BE} of Q_1 and Q_2, and the positive TC of a MOSFET, MP10, operating in the linear region. In such a situation, the TC is minimized.

3 Simulation results

The proposed low drift current reference is designed to provide current bias for a high voltage LED driver with high precision. It is designed and simulated using a CSMC 1 μm 40 V BCD process.

The supply voltage of the proposed current reference circuit is 5 V and the minimum working voltage is about 2 V. The current consumption is 5.1 μA at 27 °C with a supply voltage of 5 V.

Fig. 3 shows the simulation results of PTAT current I_{PTAT} and the output current I_{bias} over a temperature range of −40–120 °C in a typical corner. The TC of I_{PTAT} and I_{bias} are 2127×10^{-6}/°C and 23.8×10^{-6}/°C over a temperature range of −40–120 °C, respectively.

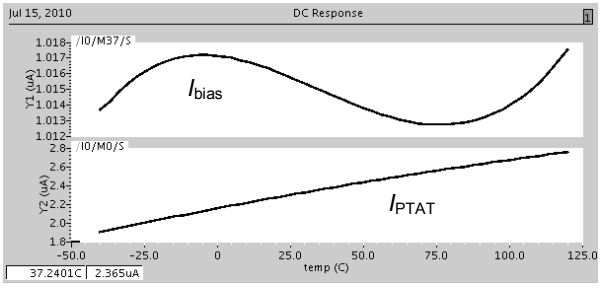

Fig. 3 Simulation results of I_{PTAT} and I_{bias} in a typical corner

Fig. 4 shows the simulation results of PTAT current I_{PTAT} and the output current I_{bias} over a temperature range of −40–120 °C in different corners. In the worst process corner, a slow corner for resistors, MOSFET, and bipolar transistors, the TC of I_{bias} is 85×10^{-6}/°C over a temperature range of −40–120 °C.

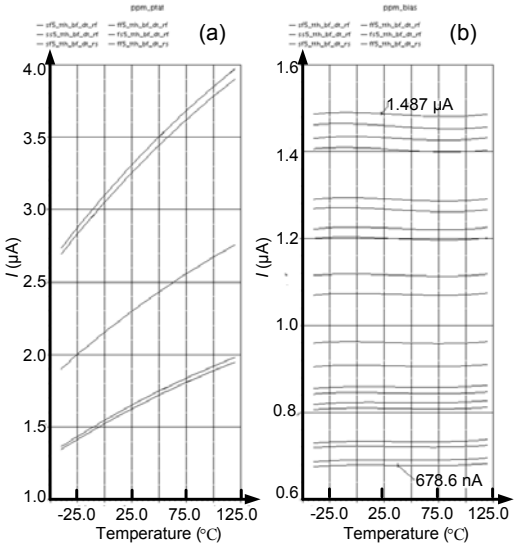

Fig. 4 Simulation results of I_{PTAT} (a) and I_{bias} (b) in different corners

Table 1 presents a comparison between our proposed current reference and some of the architectures proposed in the literature. The TC of our proposed current reference is much lower and the current consumption is quite small. Besides, compared with the current references proposed by Yoo and Park (2007), Serrano and Hasler (2008), and Yang *et al*. (2009), our proposed current reference has the simplest structure and is the easiest to design.

4 Trimming and layout

The principle and the simulation of the proposed current reference show that the mismatch of devices and process variations would deteriorate its TC property. MP10 is the main device adjusting the TC of the reference current. Therefore, MP10 is trimmed to obtain a perfect curve of the TC. According to the calculation of I_{ref}, the size of MP10 is designed to have a length larger than its width. Considering the accuracy of device parameters and for convenience of trimming, MP10 uses a series of normal PMOS (W/L=6 μm/3 μm). The downward trend of the TC curve is more marked with increase in the number of PMOSs in series. The TC curve will be optimal when

Table 1 Performance comparison of current reference

Parameter	Value/Description			
	Byung *et al*. (2009)	Yoo and Park (2007)	Serrano and Hasler (2008)	This work
Technology	0.35 μm CMOS	0.25 μm CMOS	0.5 μm CMOS	1 μm 40 V BCD
Supply voltage	2–3.3 V	1.1–3 V	2.3–3.3 V	2.5–5 V
Supply Current	N/A	70 μA	N/A	5.1 μA
Temperature range	−20–100 °C	0–120 °C	0–80 °C	−40–120 °C
Temperature drift	280×10^{-6}/°C	60×10^{-6}/°C (simulated) 720×10^{-6}/°C (measured)	$<130\times10^{-6}$/°C	23.8×10^{-6}/°C (typical) 85×10^{-6}/°C (worst)

MP10 is made of 15 PMOS in series; in such a case, however, the trimming may result in only a downward trend. In this study, MP10 is designed as a 14-PMOS series, and the trimming is designed to have 4 bits, which are 1/4, 1/2, 1, and 2. The trimming range is −6.7%–18.3%, and the trimming precision is 1.7%.

The proposed low drift current reference is fabricated in CSMC's 1 μm 40 V BCD process after we have completed the design and layout of the whole chip of a high voltage LED driver with high precision. The size of the layout of the proposed current reference (Fig. 5) is 0.18 mm×0.25 mm. The relevant pins and trimming pads are placed on the whole chip layout. The post simulation has been conducted with the parasitic parameters extracted from the layout. There is little difference between the post simulation results and the simulation results in Section 3.

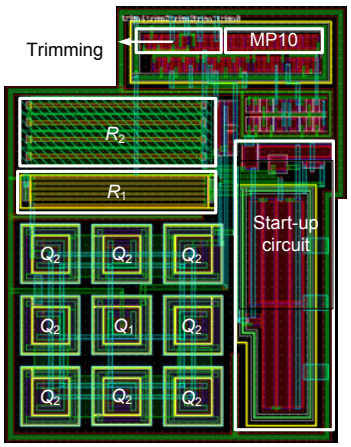

Fig. 5 Layout of the proposed low drift current reference

5 Conclusions

A low drift current reference based on PMOS temperature correction technology has been proposed. A PTAT current generating circuit is designed to produce a PTAT current. Then, a cross structure of PMOS cascode current mirror is used, forcing the upper PMOS to work in the linear region to adjust the TC of the proposed current reference, together with the resistor of the self-biased PMOS cascode structure in the PTAT current generating circuit. Therefore, the adjusted current of the proposed current reference is temperature insensitive. Simulation results show that the TC of the proposed current reference is 23.8×10^{-6}/°C in a typical corner over the temperature range of −40–125 °C. In the worst case of the process corners, the TC is 85×10^{-6}/°C over the temperature range of −40–125 °C. Moreover, MP10, the main device adjusting the TC of the reference current, is trimmed to obtain a perfect TC curve of the output current.

Compared with other current references, the proposed current reference is designed with a novel structure, fewer devices, and a simpler circuit, and has good performance.

The circuit is designed and simulated with a CSMC 1 μm 40 V BCD process. The layout has been finished and the post simulation results are similar to the simulation results in Section 3. The test chip of a high voltage LED driver with the proposed low drift current reference on chip is now being fabricated.

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