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A 31–45.5 GHz injection-locked frequency divider in 90-nm CMOS technology*

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Abstract: We present a 31–45.5 GHz injection-locked frequency divider (ILFD) implemented in a standard 90-nm CMOS process. To reduce parasitic capacitance and increase the operating frequency, an NMOS-only cross-coupled pair is adopted to provide negative resistance. Acting as an adjustable resistor, an NMOS transistor with a tunable gate bias voltage is connected to the differential output terminals for locking range extension. Measurements show that the designed ILFD can be fully functional in a wide locking range and provides a good figure-of-merit. Under a 1 V tunable bias voltage, the self-resonant frequency of the divider is 19.11 GHz and the maximum locking range is 37.7% at 38.5 GHz with an input power of 0 dBm. The power consumption is 2.88 mW under a supply voltage of 1.2 V. The size of the chip including the pads is 0.62 mm×0.42 mm.

Key words: CMOS, Injection-locked frequency divider (ILFD), Millimeter wave, Wide locking range, Monolithic microwave integrated circuit (MMIC)

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1 Introduction

With the rapid development of wireless communication, millimeter wave (mm-wave) technology has achieved significant progress due to its compensation for spectrum blockage and providing necessary satisfaction to the increasing requirements for higher data-rate transmission. To take advantage of the wide spectrum, the primary challenges of developing integrated circuits (ICs) for mm-wave applications are higher operation frequency and wider frequency coverage. In terms of phase-locked loops (PLLs) or frequency synthesizers, the design of a high-speed divide-by-two frequency divider acting as the prescaler with a wide frequency locking range has become a challenge.

Operating at high frequency with low power consumption, injection-locked frequency dividers (ILFDs) are usually used as the first divider in mm-wave PLLs (Lee *et al.*, 2008; Weng and Lu, 2012; Yu *et al.*, 2013). Nevertheless, a conventional ILFD usually suffers from the drawback of a narrow locking range. In Katz *et al.* (2011), a low-power divide-by-two injection-locked frequency divider was developed in a standard 90-nm CMOS process. The schematic of the divider is shown in Fig. 1, where a capacitor bank for divider band selection is used with a frequency locking range of 2.5 GHz achieved at an input power of 2 dBm. The locking range is too narrow when it is used in mm-wave frequency synthesizers. To extend the locking range, a modified ILFD is developed in this design (Fig. 2). Compared with the structure shown in Fig. 1, an NMOS transistor M4 with a tunable gate bias voltage V_{tune} connected to the differential output terminals is introduced in the proposed ILFD, to produce an adjustable resistance

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r_{ds} and significantly extend the locking range. The proposed divider was designed and implemented in a standard 90-nm CMOS process. Under 1 V tunable bias voltage V_{tune}, a maximum locking range from 31 to 45.5 GHz at 0 dBm input power is achieved.

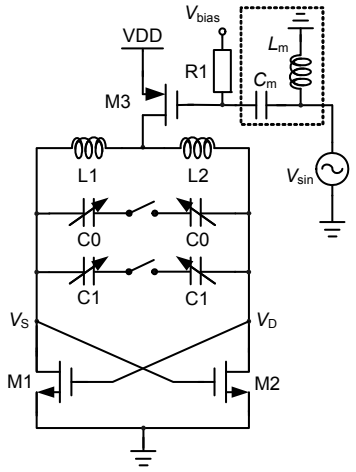

Fig. 1 Circuit schematic of the ILFD proposed in Katz *et al.* (2011)

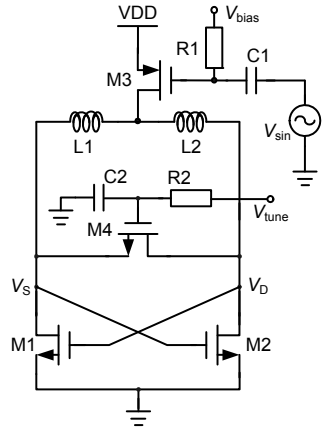

Fig. 2 Schematic of the proposed ILFD

2 Circuit design

As shown in Fig. 2, the proposed ILFD consists of a self-resonant circuit and an NMOS transistor M4 with a tunable gate bias voltage V_{tune}. Transistor M4 is connected to the differential output terminals to provide an adjustable resistor, and the locking range can be extended by adjusting V_{tune}. The input signal is injected into the gate of the tail transistor M3, and the output is locked at half the frequency of the input signal as the frequency of the input signal is close to twice the self-resonant frequency. The absence of varactors is significantly conductive to the operating frequency and locking range (Chen *et al.*, 2010).

As described in Razavi (2004), the locking range of the ILFD can be derived using the phasor analysis method. As shown in Fig. 3, the current I_{tank} flowing through the LC tank is generated by the injection current I_{inj} added to the self-resonant current I_{osc}, which remains in phase with V_D under all conditions to satisfy the Barkhausen criterion for oscillation. Fig. 4 shows the phasor diagram. A phase shift α is inserted in the loop due to the existence of injection current I_{inj}. To cancel the phase shift α and make the output voltage V_D ($I_{tank}Z_{tank}$) remain in phase with I_{osc}, the operating frequency must change from the natural resonance ω_{osc} to a new frequency ω_{inj} to produce a phase angle.

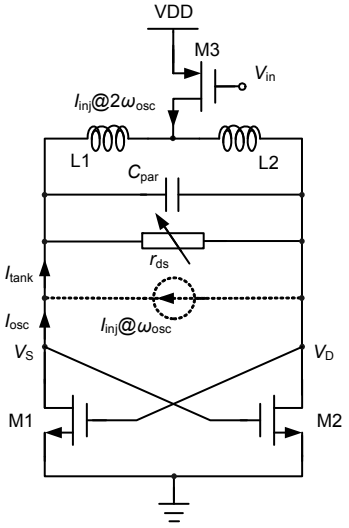

Fig. 3 Equivalent current model of the proposed ILFD

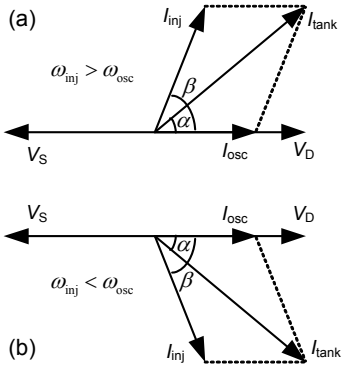

Fig. 4 Phasor diagram: (a) $\omega_{inj}>\omega_{osc}$; (b) $\omega_{inj}<\omega_{osc}$

Without small locking range approximation, the maximum locking range of the ILFD can be derived as (Katz *et al.*, 2011)

$$\Delta\omega_{\max}=2\omega_{\mathrm{o}}\cdot\left(1-\sqrt{1-\frac{\eta}{Q\sqrt{1-\eta^2}}}\right), \tag{1}$$

where ω_{o} and Q are the self-resonant frequency and quality factor of the LC tank, respectively, and η is the current injection ratio defined by the ratio of injection current to oscillation current, i.e., $\eta=I_{\mathrm{inj}}/I_{\mathrm{osc}}$.

The quality factor Q of the LC tank can be defined as

$$Q=r_{\mathrm{ds}}\sqrt{C_{\mathrm{par}}/L_{\mathrm{ind}}}, \tag{2}$$

where L_{ind} is the inductance of the LC tank, C_{par} is the parasitic capacitance stemming from the required inductance and the transistors, and r_{ds} is the channel resistance of transistor M4, defined as

$$r_{\mathrm{ds}}=\frac{1}{\mu_{\mathrm{n}}C_{\mathrm{ox}}(V_{\mathrm{gs}}-V_{\mathrm{TH}}-V_{\mathrm{DS}})W/L}, \tag{3}$$

where μ_{n} is the surface mobility of the channel for the n-channel device, C_{ox} is the capacitance per unit area of the gate oxide, V_{TH} is the threshold voltage, V_{DS} is the drain-to-source voltage of M4, V_{gs} is the gate-to-source voltage of M4, $V_{\mathrm{gs}}=V_{\mathrm{tune}}-V_{\mathrm{S}}$, and W and L are the effective channel width and length, respectively.

As a result, the locking range can be expressed as

$$\Delta\omega_{\max}=2\omega_{\mathrm{o}}\cdot\left(1-\sqrt{1-\frac{\eta\mu_{\mathrm{n}}C_{\mathrm{ox}}\left(\frac{W}{L}\right)(V_{\mathrm{tune}}-V_{\mathrm{S}}-V_{\mathrm{TH}}-V_{\mathrm{DS}})\sqrt{L_{\mathrm{ind}}}}{\sqrt{C_{\mathrm{par}}}\sqrt{1-\eta^2}}}\right). \tag{4}$$

Accordingly, due to the existence of transistor M4, an adjustable resistance r_{ds} is produced, and the maximum locking range $\Delta\omega_{\max}$ is extended by increasing the tunable gate bias V_{tune}. Fig. 5 shows the simulated injection sensitivity curves of the proposed ILFD with respect to the different bias voltages (for V_{tune}=0, 0.7, 0.9, and 1 V). The injection sensitivity is improved and the locking range is enlarged due to the increased bias voltage V_{tune}, which agrees well with theoretical analysis.

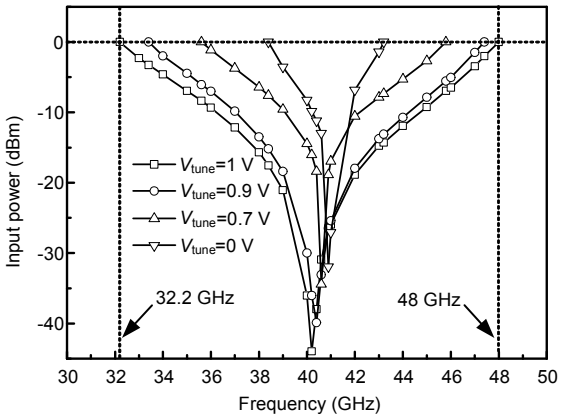

Fig. 5 Simulated input sensitivity curves for V_{tune}=0, 0.7, 0.9, and 1 V

The self-resonant frequency of the ILFD is influenced slightly by the equivalent parasitic capacitance C_{ds} of switch transistor M4. As shown in Fig. 6, when bias voltage V_{tune} is adjusted from 0 to 1 V, C_{ds} becomes large due to the increased depletion-layer capacitance C_j of M4, which can be expressed as $C_{j0}/(1-V_{\mathrm{tune}}/\phi)^m$, where ϕ is the barrier potential and m a grading coefficient, $1/3\leq m\leq 1/2$ (Allen and Holberg, 2002). As a result, the self-resonant frequency of the proposed ILFD is decreased slowly owing to the increased V_{tune}.

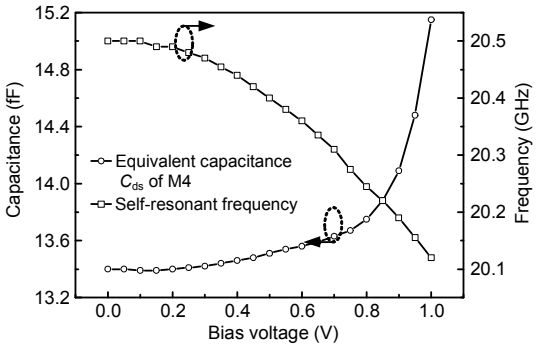

Fig. 6 Simulated equivalent parasitic capacitance C_{ds} of M4 and self-resonant frequency under different V_{tune}'s

The schematic of the proposed ILFD is as shown in Fig. 2. To reduce the parasitic capacitance and increase the operating frequency, an NMOS-only cross-coupled pair is adopted to provide the negative

resistance. A PMOS tail transistor M3 is used to provide a constant current source. The output buffer shown in Fig. 7 is used to drive the 50 Ω output load for measurements. The input signal is injected through the PMOS transistor. Since the signal is injected into the gate of M3, signal voltage swing is the main driving mechanism. In Katz *et al.* (2011), an LC matching network was adopted to maximize the input signal at the PMOS gate. The simulated input power with or without the matching network is as shown in Fig. 8. Due to the utilization of the matching network, a large input power is achieved within the matching frequency range. However, for a first-order LC matching network, a smaller matching bandwidth is achieved. When the frequency is out of the matching frequency range, the input power decreases rapidly and is lower than that without the matching network, which goes against the wide locking range. As a result, the matching network is not used in the proposed design. To produce a large injection current I_{inj} and

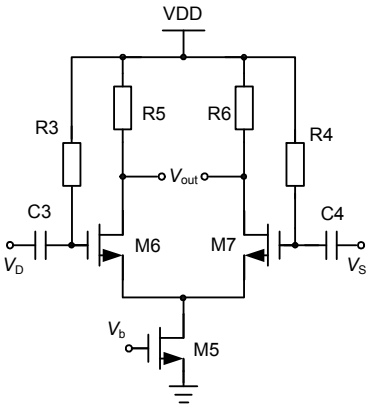

Fig. 7 Buffer schematic of the proposed ILFD

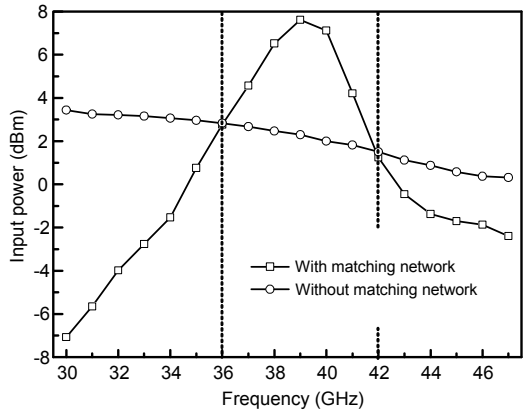

Fig. 8 Simulated input signals for the situations with or without matching network circuit

improve the locking range, a 0.5 V bias voltage V_{bias} is applied to provide a large overdriven voltage for the PMOS transistor M3. A larger gate-to-source voltage of M1 and M2 leads to a smaller size of the transistor for equal negative resistance. The parasitic capacitance is reduced and the operating frequency is further improved. Under a 1.2 V supply voltage, the dc voltage level of the differential output nodes is set at 0.65 V by properly choosing the sizes of the PMOS transistor M3 and the NMOS cross-coupled transistors M1 and M2. To obtain a wide operating range and low power consumption, the optimum width of the cross-coupled pair (M1 and M2) is 1×12 μm, and the width of the PMOS transistor M3 is 1×48 μm with a 2.2 mA core current from 1.2 V supply.

In contrast with the structure in Fig. 1, in this design, an NMOS transistor M4 with a tunable gate voltage V_{tune} is connected to the differential output terminals to produce an adjustable resistance r_{ds} in this design, and the larger bias voltage V_{tune} leads to the smaller resistance r_{ds} and wider locking range $\Delta\omega_{max}$. Nevertheless, the reduction of resistance r_{ds} decreases the output amplitude ($\propto I_{tank}r_{ds}$) of the ILFD, Furthermore, the divider would even fail to oscillate if resistance r_{ds} is less than the absolute value of negative resistance R_{neg} provided by the NMOS-only cross-coupled pair. The bias voltage V_{tune} should be chosen carefully. For special applications, V_{tune} is tuned externally for the divider to produce enough output power driving the following circuits and achieve a relatively wide locking range at the same time. In this design, the optimum width of transistor M4 is 1×28 μm. Instead of a center-tap inductor, two spiral inductors implemented simply by top metal are applied in the circuit and a 590 pH inductance is achieved to make the self-resonant core of the divider oscillate around 19 GHz.

3 Experimental results

The proposed ILFD is implemented using a 90-nm CMOS process. Fig. 9 shows the microphotograph of the chip, which occupies an area of 0.62 mm×0.42 mm. The power consumption of the core circuit is 2.88 mW at the supply voltage of 1.2 V. The proposed buffer consumes a power of 9.8 mW for driving a 50 Ω load resistance.

On-wafer measurements have been performed using an Agilent E4440A PSA 26.5 GHz series spectrum analyzer, Agilent E4448A PSA 50 GHz series spectrum analyzer, and a signal generator. The differential output signals are connected to the balun firstly and then sent to the spectrum analyzer. The measured free running frequency is 19.11 GHz under 1 V bias voltage (Fig. 10a). The locked output spectrum for a 38.5 GHz input signal is shown in Fig. 10b when the injection power is 0 dBm and the bias voltage V_{tune} is 1 V. The measured output power is −15.44 dBm with a 4.2 dB output cable loss.

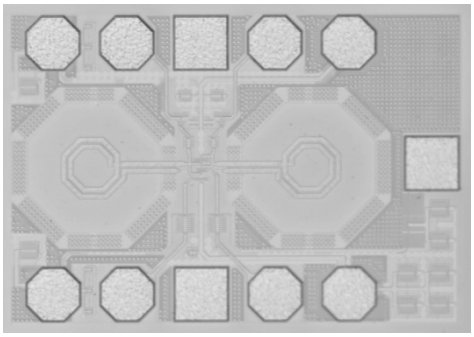

Fig. 9 Chip photograph of the proposed ILFD

Fig. 11a shows the measured injection sensitivity curves of the ILFD with respect to the different tunable bias voltages (V_{tune}=0, 0.7, 0.9, and 1 V). The injection sensitivity is improved and the locking range is enlarged as V_{tune} increases. At V_{tune}=1 V, the maximum locking range $\Delta\omega_{\max}$ covers the frequency from 31 to 45.5 GHz with 0 dBm input power. Fig. 11b shows the curves of the measured output power for different V_{tune}'s. The output power is reduced as V_{tune} is enlarged. For V_{tune}=1 V and a 50-Ω load resistance, the output power fluctuates between −18.8 and −11 dB when the input frequency varies from 30 to 46 GHz.

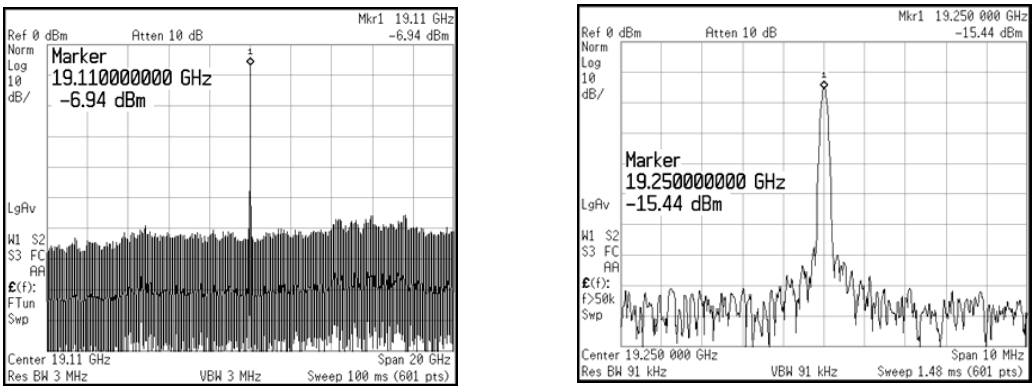

Fig. 10 Measured output spectrums: (a) self-resonant spectrum of the proposed ILFD; (b) output spectrum with a 38.5 GHz input signal

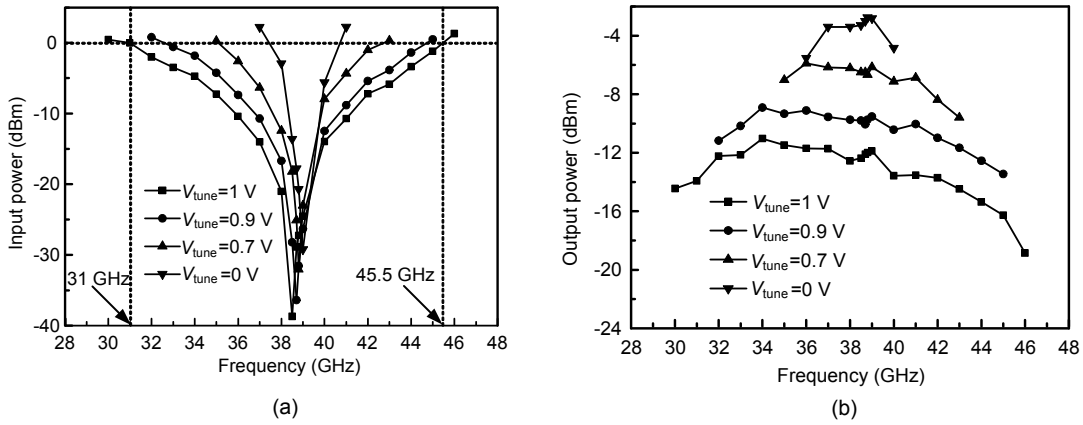

Fig. 11 Measured input sensitivity (a) and output power (b) curves for V_{tune}=0, 0.7, 0.9, and 1 V

As shown in Fig. 12, when the bias voltage V_{tune} varies from 0 to 1 V, the locking range is increased from 3.2 to 14.5 GHz, and the output power for 50-Ω load resistance decreases from −2.8 to −11.9 dBm at 0 dBm input power. For special applications, V_{tune} is tuned externally and chosen to be an apt value for the divider to produce large enough output power for the following circuits and achieve a relatively wide locking range at the same time. The simulated curves are incorporated for comparison and they correspond well with the measured ones.

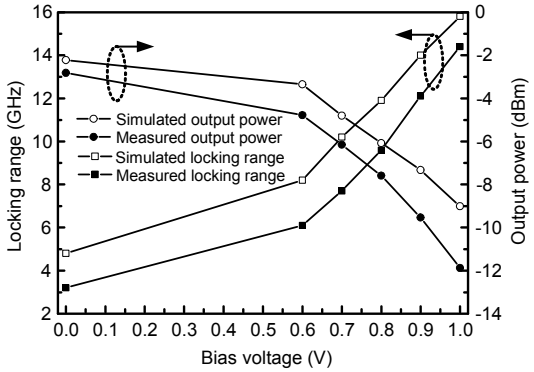

Fig. 12 Simulated and measured locking ranges and output power for different V_{tune}'s

As shown in Fig. 13, when the bias voltage V_{tune} of M4 is tuned from 0 to 1 V, the measured output phase noise at 500 kHz and 1 MHz frequency offsets is decreased insignificantly due to the reduced output power. Compared with the phase noise of the 38.5-GHz input signal, the output phase noise is lower than that of the input signal by approximately 6 dB, which corresponds well with the theoretical value. Fig. 14 shows the measured phase noise curves of the 38.5 GHz input signal and the output signal under 1 V bias voltage.

Table 1 summarizes the characteristics of the proposed ILFD and other reported mm-wave frequency dividers in terms of input power, operation frequency, locking range, power consumption, and figure-of-merit (FOM). To consider the input power provided by the preceding circuit, a modified FOM is defined by the locking range divided by the input power level and power consumption. Compared with the ILFD designed by Katz *et al.* (2011), this work achieves a wider locking range due to the introduction of M4 at a cost of larger power consumption, as well as a better FOM. The circuit proposed by Luo *et al.* (2008) shows better FOM due to lower power consumption. However, the output power is much lower and decreases rapidly when the frequency moves away from the self-resonant frequency, and a larger chip area is occupied.

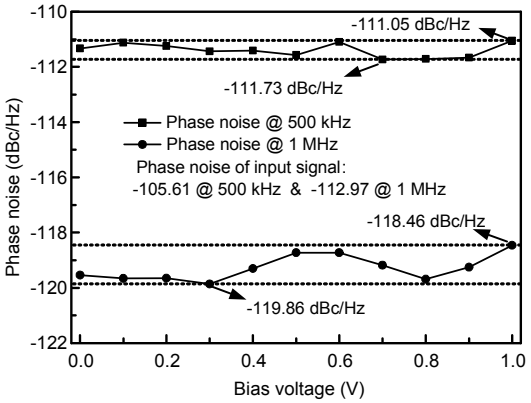

Fig. 13 Measured output phase noise under different bias voltages

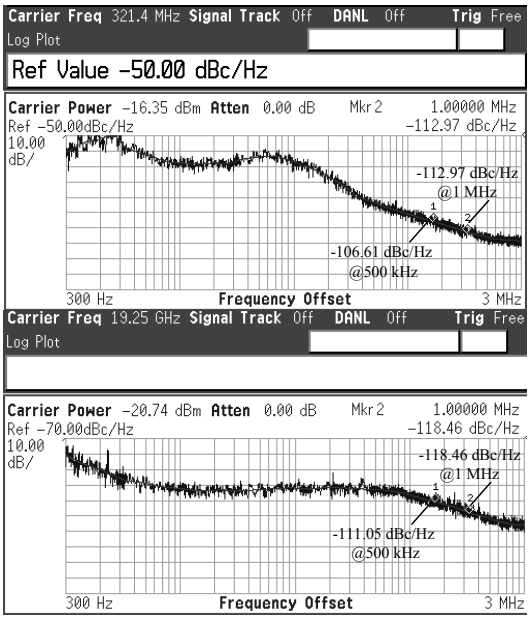

Fig. 14 Measured input (top) and output (bottom) phase noise versus frequency offset when the input signal frequency is 38.5 GHz

The input signal is sent to a 50 GHz spectrum analyzer to produce a 321.4 MHz output signal, and then the output signal is sent to a 26.5 GHz spectrum analyzer to measure the phase noise

Table 1 Comparison of the performances for the currently published frequency dividers

Parameter	Value/Description				
	This work	Katz *et al.* (2011)	Cheema *et al.* (2010)	Luo and Chen (2008)	Wang *et al.* (2011)
Process	90 nm CMOS	90 nm CMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS
Input power (dBm)	0	0	−2	0	0
Frequency (GHz)	31–45.5	67.5–70	30.3–44	39–51	52.7–62.8
VDD (V)	1.2	0.5	1.2	0.8	1.2
Power consumption (mW)	2.88	1.32	4.5	0.8	4.25
Locking range					
Absolute (GHz)	14.5	2.5	13.7	12	12.1
Relative (%)	37.7	3.64	36.9	26.1	20.5
Chip area (mm^2)	0.26	0.086**	0.675	0.39	0.083**
FOM* (GHz/mW^2)	5.04	1.9	4.83	7.63	1.42

* FOM=locking range (GHz)/(P_{DC} (mW)×P_{inj} (mW)). ** Core area

4 Conclusions

We propose an ILFD with a tunable locking range and tunable output power. An NMOS transistor with a tunable voltage V_{tune} is connected to the differential output terminals to produce adjustable resistance r_{ds}. By increasing the bias voltage V_{tune}, the frequency locking range of the ILFD is extended while the output power is reduced. For special applications, V_{tune} can be set to be an apt value for the divider to produce large enough output power and achieve a relatively wide locking range. The ILFD is fabricated using a standard 90-nm CMOS process and the overall chip area is 0.62 mm×0.42 mm. At 1 V tunable voltage, a total locking range of 37.7% is achieved at 38.5 GHz with the incident power of 0 dBm. Compared with the reported CMOS mm-wave frequency dividers, the proposed ILFD achieves the widest locking range. The divider consumes 2.88 mW power at 1.2 V supply voltage. A good FOM, defined as the ratio of the locking range to the power consumption and input power level, is achieved.

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