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A 37 GHz wide-band programmable divide-by-*N* frequency divider for millimeter-wave silicon-based phase-locked loop frequency synthesizers*

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Abstract: A 37 GHz wide-band programmable divide-by-*N* frequency divider (FD) composed of a divide-by-2 divider (acting as the first stage) and a divider with a division ratio range of 273–330 (acting as the second stage) has been designed and fabricated using standard 90 nm CMOS technology. The second stage divider consists of a high-speed divide-by-8/9 dual-modulus prescaler, a pulse counter, and a swallow counter. Both the first stage divider (with high speed) and the divide-by-8/9 prescaler employ dynamic current-mode logic (DCML) structure to improve the operating performance. The first stage divider can work from 2 to 40 GHz and the whole divider covers a wide frequency range from 25 to 37 GHz. The input sensitivity is as low as −20 dBm at 32 GHz and the phase noise at 37 GHz is less than −130 dBc/Hz at an offset of 1 MHz. The whole chip dissipates 17.88 mW at a supply voltage of 1.2 V and occupies an area of only 730 μm ×475 μm.

Key words: Wide-band, Divide-by-*N*, Frequency divider, Dynamic current-mode logic (DCML), Pulse and swallow counters, CMOS

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1 Introduction

Frequency dividers (FDs) are essential blocks of phase-locked loops (PLLs) in conventional millimeter-wave (mm-wave) transmitter/receivers and radio frequency applications (Cheema *et al*., 2010; Hammad *et al*., 2010; Gai *et al*., 2011). The proposed wide-band programmable divide-by-*N* FD is designed to be used in a 27.3–33 GHz CMOS PLL which will be used in an Atacama large millimeter/submillimeter array (ALMA) band-1 (31.3–45 GHz) silicon-based imaging system. This band was not selected for construction during the initial phase of the project, despite being declared a high scientific priority by the ALMA Scientific Advisory Committee. As a result, this band is less explored and challenging to develop (Cheema *et al*., 2010; Reyes *et al*., 2010; Gai *et al*., 2011).

In this study, a 37 GHz wide-band programmable divide-by-*N* FD was designed and fabricated using TSMC standard 90 nm CMOS technology. In this design, a divide-by-2 pre-divider (acting as the first stage) and a divider with a division ratio range of 273–330 based on pulse/swallow (P/S) counters (acting as the second stage) have been used to generate a 50 MHz output signal for a phase frequency detector (PFD) and a charge pump (CP), the next stage of FD development in PLL. To increase the operating frequency range of the first stage divider, an

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advanced dynamic current-mode logic (DCML) divide-by-2 FD was proposed which can work at an operating frequency of from 2 to 40 GHz at a supply voltage of 1.2 V. Through an external bias voltage calibration technique, this divide-by-2 FD achieves the widest operating frequency range among all published divide-by-2 FDs at an input sensitivity of lower than 0 dBm (Wong *et al*., 2005; Usama and Kwasniewski, 2006; Luo and Chen, 2008). The second stage FD employs a high-speed divide-by-8/9 dual-modulus prescaler, a P counter, and an S counter. A DCML latch with tail current source was used in this divide-by-8/9 divider which is of low-power consumption. To eliminate glitches associated with traditional divide-by-8/9 dividers, a true single-phase clock (TSPC) based D-flip-flop (DFF) latch was added. The proposed divider covers a wide frequency range of from 25 to 37 GHz and dissipates a maximum power consumption of 17.88 mW at a supply voltage of 1.2 V, including buffer and bias power consumption. The phase noise for a 37 GHz input is −132.146, −135.760, −132.026, and −135.038 dBc/Hz at division ratios of 556, 588, 652, and 620, respectively, with an offset of 1 MHz. The input sensitivity is very high. So, the minimum input power is only −20 dBm at 32 GHz at a supply voltage of 1.2 V. The chip occupies an area of 730 μm×475 μm.

The presented FD, to the best of our knowledge, is a programmable FD based on the CMOS pulse and swallow counters. It is with the widest frequency range at a supply voltage of 1.2 V below an input power of 0 dBm, which can be used in mm-wave PLL applications. When the input signal is set less than 0 dBm, which applies to integrated systems, the first stage FD is able to work in a frequency range of from 3 to 40 GHz and the second stage FD achieves a consecutive programmable division ratio frequency modulation of from 273 to 330.

2 Millimeter-wave programmable FD architectures

2.1 Architectures based on different first stage FDs

One of the most critical blocks in a PLL is the first stage of the frequency divider, because it will greatly influence the performance of the whole PLL system. Structures of mm-wave programmable FDs can be divided into current-mode logic (CML) divider based and injection-locked frequency divider (ILFD) based structures according to the first stage divider's structure which follows the voltage controlled oscillator (VCO).

Due to speed requirements, injection-locked divide-by-2 divider is typically used as the first stage of an FD in an mm-wave PLL (Luo and Chen, 2008; Pellerano *et al*., 2008; Chen *et al*., 2011; Murphy *et al*., 2011). Fig. 1a shows a PLL block diagram of an ILFD-based structure, i.e., mm-wave programmable FD (Pellerano *et al*., 2008). It uses a divide-by-4 ILFD which can reduce power consumption compared to a divide-by-2 FD. Although a digital calibration technique was implemented to overcome the ILFD locking-range limitations, the locking-range is still as low as 1 GHz.

Compared to an ILFD-based mm-wave programmable FD, a CML divider based mm-wave programmable FD is a good alternative because of its wide input frequency range (Wong *et al*., 2005; Usama and Kwasniewski, 2006). Fig. 1b shows the proposed CML mm-wave programmable FD, which provides both a wide working range and a small chip

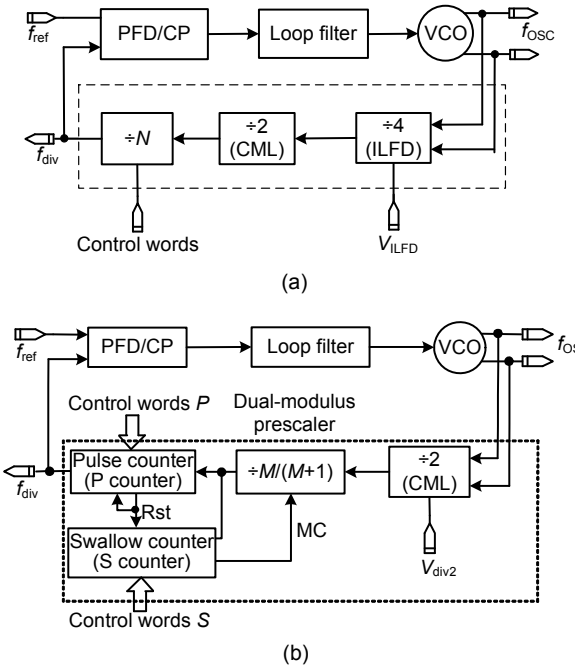

Fig. 1 Millimeter-wave PLL structures with different first stage FDs

(a) An ILFD-based structure; (b) Our proposed CML FD-based structure

area. Compared to the structure, the first stage FD of which is based on the normal CML, this structure uses only a small chip area for rare usage of passive devices in core circuits. It adopts only a pair of inductors in the buffer of the DCML divide-by-2 divider to enhance the dividing frequency and impedance to drive the divide-by-8/9 dual-modulus prescaler. Compared to the structure in Fig. 1a, the structure shown in Fig. 1b allows a wider working frequency range for the use of the DCML divide-by-2 divider after the VCO. This DCML divide-by-2 FD is able to work from 2 to 40 GHz compared with only a 19.2 GHz locking range of an injected-locked structure reported recently (Luo and Chen, 2008).

2.2 Architectures based on a fixed-modulus divider chain or P/S counters

A fixed-modulus divider chain based FD shares a fixed-modulus divider of each stage. Thus, all the division ratios are fixed (Ding and Kenneth, 2007; Pellerano *et al*., 2008; Gai *et al*., 2011; Murphy *et al*., 2011). Fig. 2a shows the circuit implementation of an mm-wave FD based on a fixed-modulus divider chain (Ding and Kenneth, 2007). Following the divide-by-4/5 synchronous prescaler, there is a divide-by-64 asynchronous circuit resulting in a cascading of six divide-by-2 dividers. This FD has an 8-modulus prescaler, which can realize a division ratio of 256–263 using resistor load CML flip-flops. This structure achieves high operating frequency, while maintaining a wide frequency range and a small chip area. However, its limitation is that the maximum frequency division ratio is limited by the prescaler which cannot work at high frequencies with many division ratios.

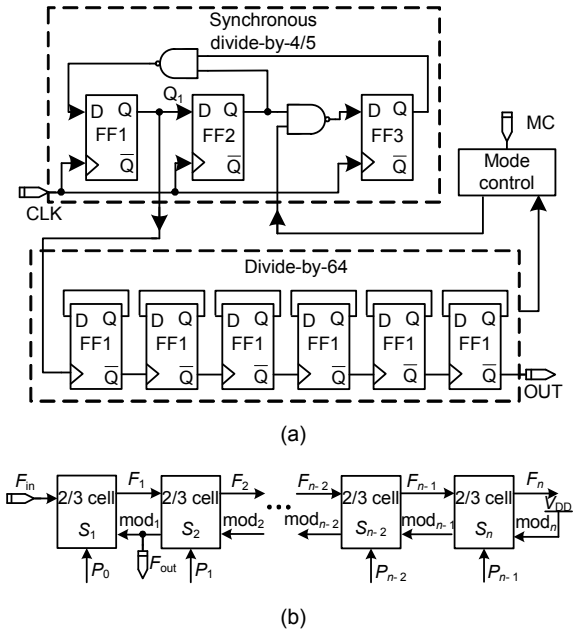

Fig. 2 Programmable FD based on a second stage FD
(a) A fixed-modulus divider chain based FD; (b) A 2/3 divider chain based FD

In contrast to a fixed-modulus divider chain based FD, there is another divider chain based FD (Fig. 2b) (Vaucher *et al*., 2000). The whole FD consists of a chain of divide-by-2/3 cells which is programmable. This structure can realize programmable integer division ratios ranging from 2^N to $2^{N+1}-1$ ($N\geq 1$). There are two advantages of this structure: (1) The feedback lines are present only between adjacent cells; (2) The topology of different 2/3 cells is the same, thereby facilitating layout work. This structure is becoming popular but still has disadvantages. For example, it is hard to design the first stage of the FD when it works in mm-wave applications.

Compared with the two FDs described above, a typical pulse and swallow counters based mm-wave FD usually consists of a dual-modulus synchronous prescaler, a P counter, and an S counter which can realize programmable divide-by-N modulation (Sheng *et al*., 1991; Jau *et al*., 2006; Gao *et al*., 2010) (Fig. 1b). The working principle is briefly described as follows: The bits of control words of the S and P counters are input signals to set the division ratio of the whole FD. At the beginning, the divide-by-M/(M+1) dual-modulus prescaler is in a high mode state (divide-by-(M+1)); the input signal F_{in} is divided by M+1 and output via F_{out}; and the S and P counters count the output of F_{out} simultaneously. When S impulses pass, the S counter reduces to 0, and the output of the S counter via the mode control signal MC changes to a low level from a high level. Thus, the M/(M+1) dual-modulus prescaler turns to a low-mode state (divide-by-M). Then the P counter continues to count. After a period of P/S impulses, a high level impulse is output to initiate the P counter. The S and P counters start to count again, and the M/(M+1) dual-modulus FD is reset to the original state to start the next cycle. The frequency division ratio of the second stage FD is

$$N'=S(M+1)+M(P-S)=PM+S, \quad (1)$$

where P and S are the numbers of the pulse and swallow counters, respectively. The divide-by-M/(M+1) dual-modulus prescaler uses P/S technology, combing the dual-modulus prescaler with a low-speed programmable controlled FD to form a stored programmable controlled P/S frequency divider with a higher speed.

In an mm-wave PLL, the power consumption of an FD based on 2/3 cells would be much higher for the use of a CML structured DFF chain. However, in a P/S counter based FD, the main power consumption part is the divide-by-M/(M+1) dual-modulus prescaler, which consists of CML latches in just one cell. So, the total power consumption would be much lower.

3 Design of millimetter-wave wide-band programmable divide-by-*N* FD circuit

Fig. 3 shows the structure of the proposed mm-wave programmable divide-by-N FD. It is designed to be used in the feedback loop of a 27.3 to 33 GHz PLL frequency synthesizer (Fig. 1b). The internal structure of the proposed FD is composed mainly of two parts: a divide-by-2 FD acting as the first stage and an FD including a divide-by-8/9 dual-modulus prescaler and P/S counters acting as the second stage. Here, the P counter has an input of six bits while the S counter has an input of three bits. The key design issues are the divide-by-2 FD which can realize a wide division range of from 2 to 40 GHz, and the modified divide-by-8/9 FD which can operate above 10 GHz. A differential buffer was also adopted following the divide-by-2 FD to prevent second harmonic generations and enlarge the output signal, which can greatly increase the sensitivity of the divide-by-8/9 FD. The proposed programmable counters are also able to operate at GHz frequency with low power consumption using TSPC DFFs.

3.1 Divide-by-2 pre-divider with buffer and external calibration block

The divide-by-2 works at the highest frequency and is the most challenging block of the two-stage FD. The operating frequency range of this block will greatly influence the range of the whole FD, while the input sensitivity is the key issue limiting the VCO performance of the PLL system. Fig. 4 shows the principle of this dynamic load CML divide-by-2 FD with frequency calibration and two stage buffer used in the first stage FD. Traditional resistor loads of static CML divide-by-2 FD are replaced by dynamic loads. Unlike Razavi's DCML topology proposed by Wong *et al.* (2005), this divider uses an external calibration block to realize fine adjustment set by the

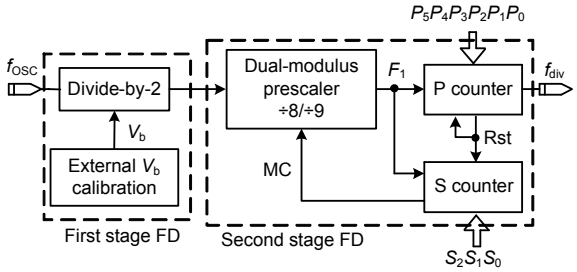

Fig. 3 Structure of the proposed FD

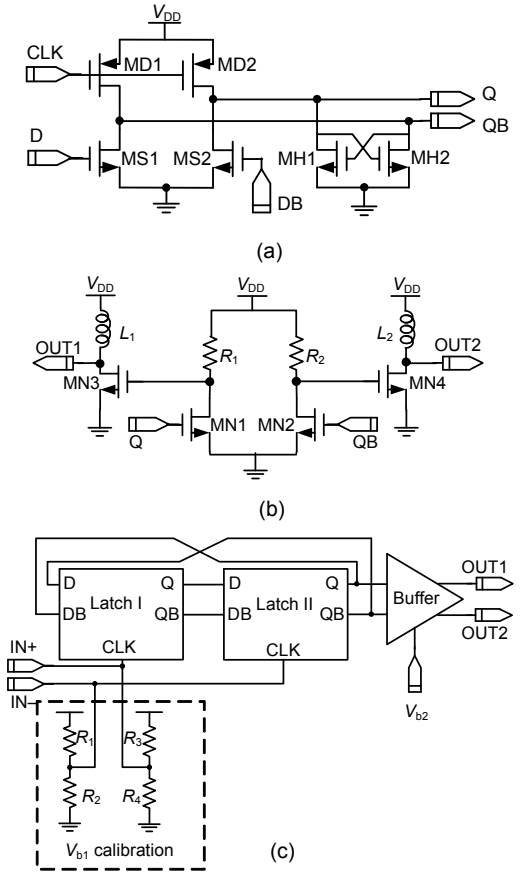

Fig. 4 Structure of the proposed first stage FD
(a) Latch; (b) Differential buffer; (c) Divide-by-2 FD with V_b calibration and buffer

bias voltage V_b and to obtain different self-resonating frequencies so that the divider is able to work in a wider frequency range. This calibration unit can also be integrated into a power management unit if it is designed on a chip.

This divide-by-2 FD which is based on CML also achieves high input sensitivity and low power consumption due to the use of dynamic loads which are changed with V_b and the clock. There are two CML latches in the key circuit. Each latch consists of a pair of dynamic loads (MD1, MD2) driven by differential clock signals, a pair of sample devices (MS1, MS2), and a pair of regenerative hold devices (MH1, MH2). In contrast to static CML topologies, the dynamic CML FDs use positive MOS (PMOS) devices as variable resistance loads instead of pure resistance loads. This improves the operating performance and avoids the problem of choosing an appropriate pure resistance load as used in static CML topologies (Guo *et al*., 2012). A two-stage differential buffer (Fig. 4b), with a pair of resonating inductors, was adopted to prevent second harmonic generation and boost the output signal. This can greatly increase the sensitivity of the divide-by-8/9 prescaler.

3.2 Divide-by-8/9 prescaler

The divide-by-8/9 prescaler is the most critical unit to achieve the programmable division ratio function (Yang *et al*., 1997; Wang *et al*., 2012). An 8/9 prescaler typically consists of a divide-by-4/5 synchronous divider, a divide-by-2 asynchronous divider, and a feedback logic section (Fig. 5). The 4/5 MC signals control how many DFFs the prescaler input signal must travel through, and therefore determine the division ratio. When the 4/5 MC signal is held low, the divide-by-4/5 synchronous cell divides the input signal by four. The signal then travels through the asynchronous divide-by-2 circuit, resulting in a total division ratio of eight. If the 4/5 MC signal is high, the divide-by-4/5 divider will divide the input signal by five. Once feedback is produced, the division ratio of the divide-by-4/5 divider is modulated to nine. An added latch 'DFF5' is used to lock the MC signal and 4/5 output signal to prevent the generation of glitches in this high speed. Then the whole pulse counting number will be added by one and the division ratio N' is modified to

$$\begin{aligned} N' &= 8(P_i+1)+S_i \\ &= 8[(P_5P_4P_3P_2P_1P_0)_B+1]+(S_2S_1S_0)_B, \end{aligned} \quad (2)$$

where 'B' denotes that the value is represented in a binary form. To enhance the divide-by-4/5 output, a three-stage buffer was used between the divide-by-4/5 synchronous divider and the divide-by-2 asynchronous divider. To better balance the propagation delays among the four latches, the output of the first flip-flop was used to drive the asynchronous divider, because the second flip-flop output drives both the first and third flip-flops.

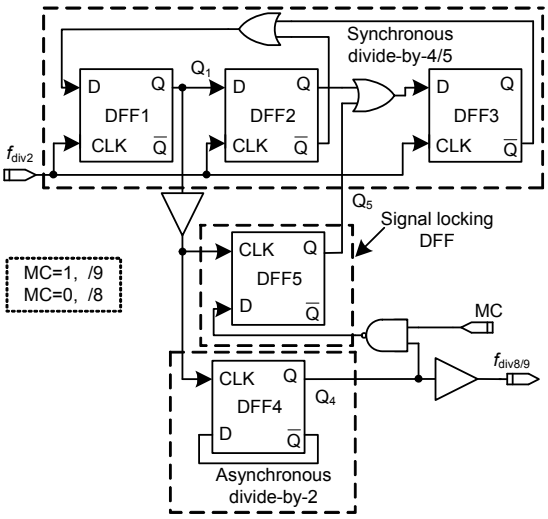

Fig. 5 Structure of the proposed divide-by-8/9 prescaler

As the divide-by-4/5 divider is the most crucial part of the whole divide-by-8/9 FD and the propagation delay through these flip-flops and NOR gates sets the maximum operating frequency in this prescaler, high performance dynamic CML DFFs (Fig. 6) were designed to realize the high working frequency (above 16.5 GHz). Fig. 6a shows the dynamic CML flip-flop structure of DFF2. To reduce the gate delay, the NOR gate and flip-flops DFF1/DFF3 were integrated as an NOR-DFF so that the operating speed can be enhanced (Fig. 6b). TSPC DFFs (Fig. 6c) were adopted in the divide-by-2 asynchronous divider (DFF4) and the signal locking DFF (DFF5). By using the modified dynamic DFFs, this divide-by-8/9 divider achieves low power consumption and high input sensitivity and operating frequencies without employing any passive devices.

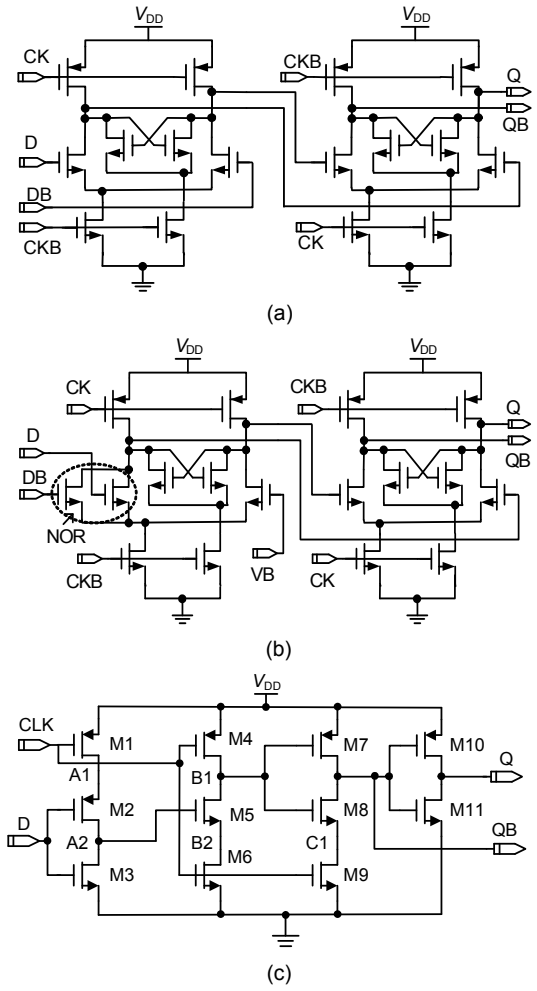

Fig. 6 Structure of DFFs used in this divide-by-4/5 prescaler

(a) Dynamic CML DFF; (b) Dynamic CML DFF with NOR; (c) TSPC DFF

3.3 Programmable pulse and swallow counters

Fig. 7 shows a schematic of the programmable pulse counter and swallow counter, both of which are based on a subtractor which sets and counts again after it reduces to 0. The S counter is more complex, and needs logic circuits equivalent to some switchers to lock up the signal and stop the S counter from working after it counts the period of S counter and awaits the next signal LD to work again. DFFs are the kernel module of the two parts which can be set and cleared synchronously. The most widely used DFF is the TSPC DFF (Eschenko *et al*., 2007). Based on the conventional TSPC structure (Fig. 6c), a TSPC DFF with a load function (Fig. 8) employs some gates on the foundation of the traditional TSPC DFF to enable it to be set and cleared at a high level.

4 Measurement results

The proposed 37 GHz wide-band programmable divide-by-*N* frequency divider was realized in a TSMC 90 nm CMOS process at a supply of 1.2 V and was tested on a wafer. To minimize the whole chip area while considering system modulation, we set P/S control words P_2/P_1 to be externally adjustable in the whole FD system and separately verified the programmable P/S counters' function when the control words P_3/S_1 were externally adjustable to obtain detailed operation and performance data. Fig. 9 shows a die photograph of this 37 GHz divide-by-*N* frequency

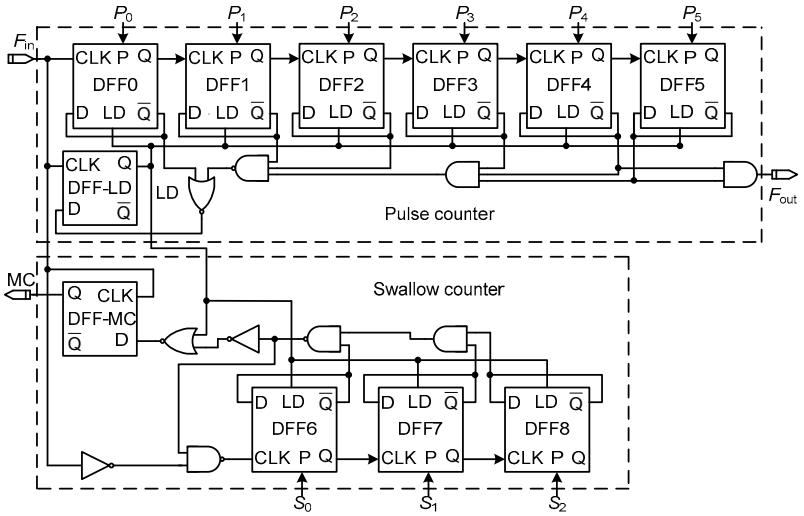

Fig. 7 Structure of the proposed programmable P/S counters

divider. The pad-limited die size is 730 μm×475 μm. Input signals were generated by an Agilent E8257D analog signal generator (Agilent, USA, ranging from 250 kHz to 40 GHz), and results were monitored using a Tektronix MSO72004C 20-GHz mixed signal oscilloscope (Tektronix, USA) and an Agilent E4448A spectrum analyzer (Agilent, USA).

4.1 Divide-by-2 frequency divider with calibration block and buffer

A single divide-by-2 FD with frequency modulation and two-stage output buffer was tested on a wafer. This FD achieves a wide operating frequency range (from 2 to 40 GHz) by using background calibration. The input bias voltage V_b is carried out off the chip to set the bias voltage to perform at four operation phases as follows: (1) During phase one, the direct analog output self-resonance frequency is 6 GHz with a current consumption of 1.5 mA; (2) During phase two, the frequency is 18 GHz with a current consumption of 4.3 mA at V_b=330 mV; (3) During phase three, the frequency is 30 GHz with a current consumption of 6.4 mA at V_b=100 mV; (4) During phase four, the frequency is 37 GHz with a current consumption of 7.3 mA at V_b=10 mV. When this FD works up to 40 GHz, the tested current is 0.8 mA and thus, the maximum power consumption is 0.96 mW. Comparisons of the performance of similar divide-by-2 CML FDs under an input power of 0 dBm are shown in Table 1. Though the FD proposed by Wong *et al*. (2005) can work from 4 to 44 GHz, when it works at an input frequency lower than 24 GHz, the input power significantly increases. According to the simulation results, the proposed divide-by-2 FD is able to work at even higher frequencies (e.g., higher than 40 GHz). However, only a frequency of 40 GHz was tested because the E8257D signal generator can provide only a highest frequency signal of 40 GHz. The use of low threshold PMOS and negative MOS (NMOS) devices improves the operating frequency. The only shortcoming of this FD is the power consumption, which is higher than those using normal threshold CMOS devices. Fig. 10 shows the sensitivity curve of this divide-by-2 divider. In Table 1, the test results are summarized and compared with other similar FDs.

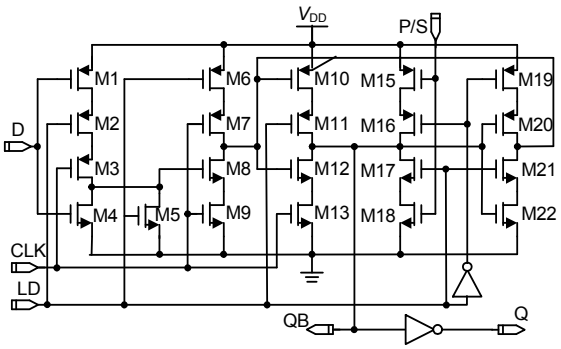

Fig. 8 The proposed TSPC DFF with load function

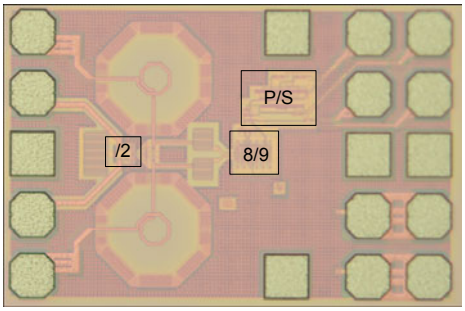

Fig. 9 Die photograph of the proposed 37-GHz divide-by-*N* FD

4.2 Programmable P/S counters with TSPC divide-by-2

Unlike that in P_2/P_1 system resolution, the control words are set to P_3/S_1 in a P/S counter testing to verify the function of both the P and S counters. To test the feedback of the MC signal and the P/S counters with the proposed input load, the input frequency was first divided by a TSPC divide-by-2 divider and put through the P/S counters. P_3/P_0 and S_1/S_0 are two

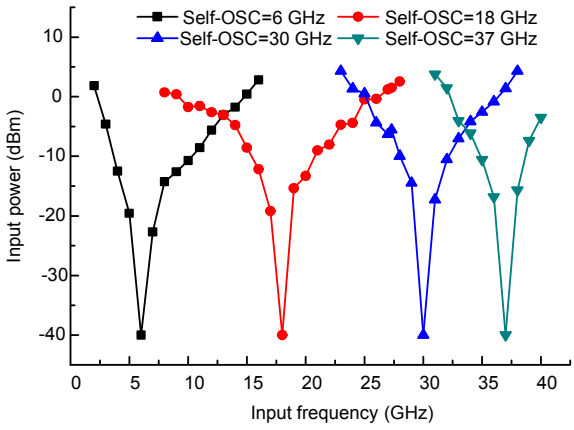

Fig. 10 The proposed divide-by-2 FD's sensitivity curve at 1.2 V

Table 1 Performance summary and comparison

Parameter	Value/Description				
	Wong *et al*. (2005)	Wong *et al*. (2005)	Usama and Kwasniewski (2006)*	Guo *et al*. (2012)	This work
Supply (V)	1.2	1–1.35	1–1.2	1.2	1.2
Structure	Static CML	Dynamic CML	Static CML	Dynamic CML	Dynamic CML
Power dissipation (mW)	5.28	2.97	0.9	1.22	0.96
Maximum frequency (GHz)	44	37	41	27	40
Division ratio	/2	/2	/2	/2	/2
Locking range (GHz)	20	20	37	20	38
Process (nm)	90	90	90	90	90

* Simulation results

pairs of invert signals which are modified at the same time to obtain widely modified P counting numbers and continuously modified S counting numbers. However, we can still achieve the worst control situation $P_5P_4P_3P_2P_1P_0/S_2S_1S_0$=100001/101 when changing four control words synchronously. Fig. 11 displays the output waveforms and spectrum at an input of 4.7 GHz when $P_5P_4P_3P_2P_1P_0/S_2S_1S_0$=100001/101.

Table 2 lists the output frequencies when P_3 was set to 0 or 1 and the MC pulses number was set according to the change of S_1. These measured results show that the programmable counting unit can successfully divide by division ratios set by P and S control words.

Table 2 List of outputs when P and S control words were modified at 4.7 GHz

$P_5P_4P_3P_2P_1P_0/S_2S_1S_0$	Division ratio $2\times(P+1)$	Theoretical frequency (MHz)	Measured frequency (MHz)	MC pulse number*
100001/101	2×34	69.1176	69.118	5
101000/110	2×41	57.3171	57.318	6

* Count value of S counter

4.3 A 37 GHz programmable divide-by-*N* frequency divider

At the whole FD clock input, the impedance of the external bias voltage calibration block was designed to match the characteristic impedance of the measurement system. At P/S control word inputs, an internal series resistance and a three-stage inverter were employed to eliminate control words witching glitches. The outputs are buffered using the three-stage inverter chains to provide sufficient voltage swing across a 50-Ω load. This 37 GHz divide-by-*N* frequency divider achieves a maximum core power consumption of 17.88 mW at a supply of 1.2 V. The input signal was provided by two 40 GHz signal generators and the outputs were measured using an oscilloscope and a spectrum analyzer. Error monitoring pads were set in the second pad row on the right side of the chip. Fig. 12 shows the output waveform and spectrum when the input frequency

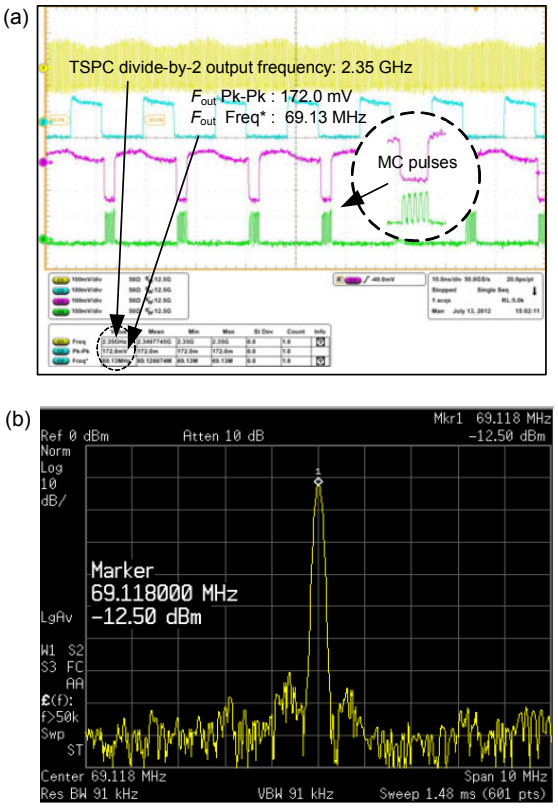

Fig. 11 The proposed FD's output waveforms and spectrum at 4.7 GHz when $P_5P_4P_3P_2P_1P_0/S_2S_1S_0$=100001/101
(a) Output waveforms; (b) Output spectrum

was the highest (e.g., 37 GHz), while Fig. 13 shows the output when the input frequency was the lowest (25 GHz), when P_2P_1 were set to 00 with a division ratio of 278. Tables 3 and 4 list the output frequencies when P_2P_1 were set to 00, 01, 11, or 10, corresponding to the division ratios 278, 294, 326, or 310 at 37 GHz and 25 GHz, separately. These measurement results show that the proposed FD can successfully divide by division ratios set by P control words. S counter control words $S_2S_1S_0$ were fixed to 110 and six pulses were monitored from the port of the MC signal (Figs. 12 and 13).

Fig. 14 shows the relationship between the input sensitivity and input frequency measured at a supply of 1.2 V. The operating frequency of the FD spans a range of 11 GHz for an input power of 0 dBm, or for a peak-peak input voltage of 0.6 V, and the input power is only −20 dBm at 32 GHz. Due to the calibration block, the output center frequency changes three times. This is reflected in Fig. 14 by three changes in the peak, which indicates that a wider working frequency range can be achieved. Because this FD was designed to be used in an ALMA band-1 27.3–33 GHz PLL, the phase noise was also monitored.

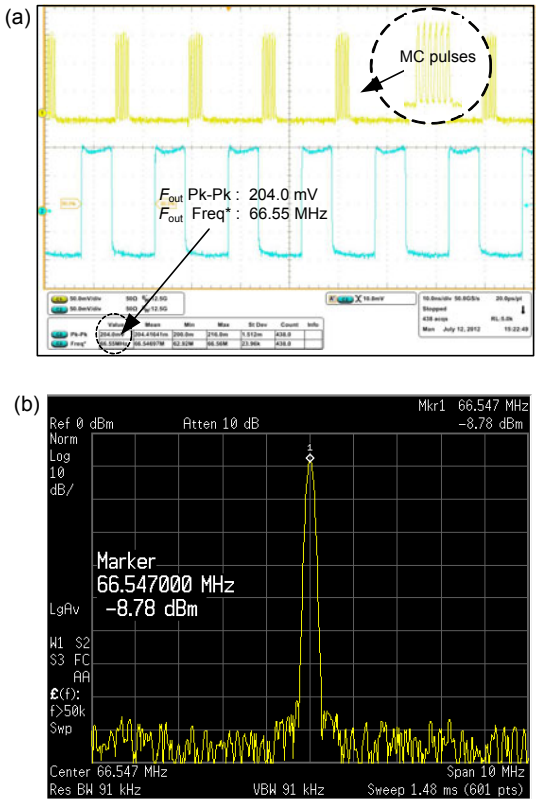

Fig. 12 The proposed FD's output waveforms and spectrum at 37 GHz when P_2P_1 is 00
(a) Output waveforms; (b) Output spectrum

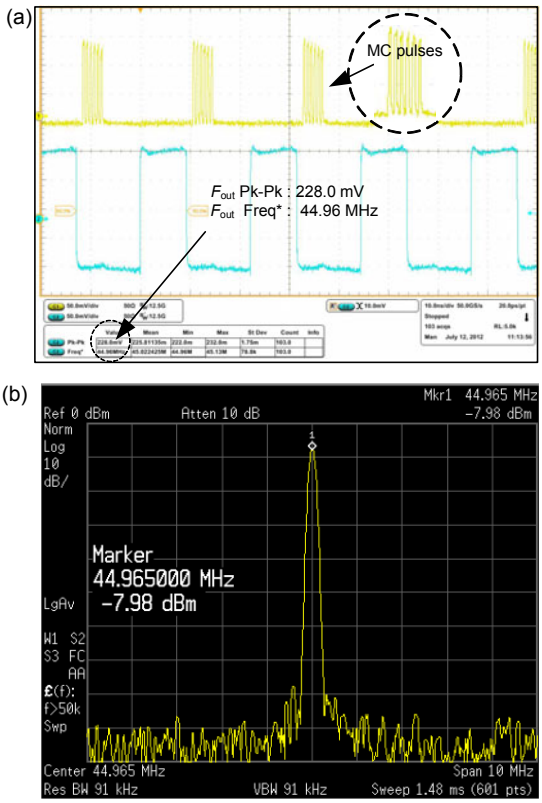

Fig. 13 The proposed FD's output waveforms and spectrum at 25 GHz when P_2P_1 is 00
(a) Output waveforms; (b) Output spectrum

Table 3 List of output frequencies at 37 GHz when $P_5P_4P_3P_0/S_2S_1S_0$ is fixed to 1001/110

P_2P_1	Output frequency (MHz)	
	Theoretical	Measured
00	37 GHz÷2÷278=66.5468	66.547
01	37 GHz÷2÷294=62.9252	62.926
11	37 GHz÷2÷326=56.7485	56.749
10	37 GHz÷2÷310=59.6774	59.678

Table 4 List of output frequencies at 25 GHz when $P_5P_4P_3P_0/S_2S_1S_0$ is fixed to 1001/110

P_2P_1	Output frequency (MHz)	
	Theoretical	Measured
00	25 GHz÷2÷278=44.9640	44.965
01	25 GHz÷2÷294=42.5170	42.517
11	25 GHz÷2÷326=38.3436	38.350
10	25 GHz÷2÷310=40.3226	40.327

Fig. 15 gives the phase noise spectrum at 37 GHz, which is the worst situation across the frequency range at division mode /278. When P_2P_1 was changed to 01, 11, or 10, the phase noise at 37 GHz input was tested to be −135.760, −132.026, and −135.038 dBc/Hz at division ratios 294, 326, and 310, respectively, at an offset of 1 MHz with a resolution bandwidth of 10 kHz.

4.4 Comparison and summary of measurements

The measurements above show that the proposed 37 GHz FD is able to work at a supply power of 1.2 V with a frequency range of 11 GHz under an input power of 0 dBm. It is able to work at any division ratio from 273 to 330 by modifying P and S control words. Moreover, it is an mm-wave frequency divider and the performance comparison between this FD and other CMOS millimeter-wavelength FDs is summarized in Table 5. There are various kinds of FD topologies used in PLL systems, but this FD allows for lower power consumption, more division ratios, and a wider frequency range. Also, as no passive devices are used in kernel circuits, the die area is conserved and it is good for digital integration.

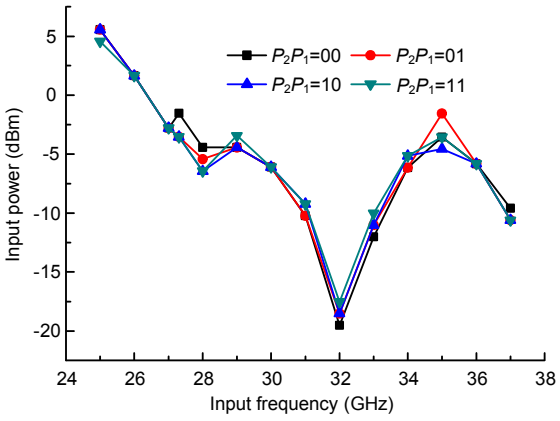

Fig. 14 Measured input sensitivity at a supply of 1.2 V

5 Conclusions

In this paper, a 37 GHz wide-band programmable divide-by-*N* FD with low power consumption is proposed. Analyses show that the proposed divider covers a wide frequency range (from 25 to 37 GHz) and dissipates a maximum power consumption of 17.88 mW at a supply voltage of 1.2 V, including buffer and bias power consumption when working at 37 GHz. The locking range is 25 to 37 GHz and is wide enough to cover 27.3 to 33 GHz ALMA band-1 PLL integration. When input signal power from the VCO is less than 0 dBm, the frequency range is as wide as 11 GHz (from 26 to 37 GHz) with a division ratio from 546 to 660. The phase noise for a 37 GHz input is −132.146, −135.760, −132.026, and −135.038 dBc/Hz at four tested division ratios of 278, 294, 326, and 310, respectively, at an offset of 1 MHz. The input sensitivity is very high given that the minimum input power is only −20 dBm at 32 GHz at a supply of 1.2 V. This chip occupies an area of only 730 μm×475 μm. In addition, the proposed divide-by-2 FD (acting as the first stage) has its widest

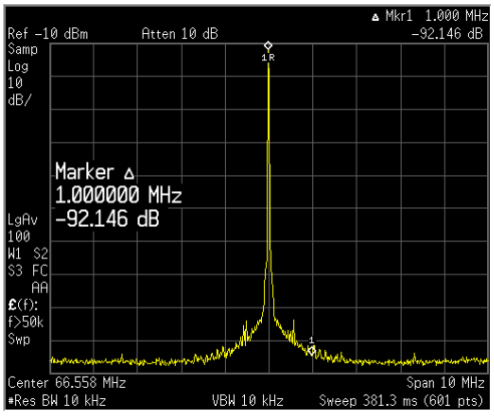

Fig. 15 The proposed FD's phase noise spectrum at 37 GHz when P_2P_1 is 00

Table 5 Performance summary and comparison

Parameter	Ding and Kenneth (2007)	Pellerano *et al*. (2008)	Chen *et al*. (2011)	This work
Supply (V)	1.5	1.2	1.5	1.2
Power dissipation (mW)	9.075	–	–	17.88
Maximum frequency (GHz)	21	41.6	41.2	37
Input power (dBm)	0	–	–	0
Division ratio	8	512–2032	512	546–660
Locking range (GHz)	14.78	2.5	1.5	11
Process (nm)	130	90	90	90

frequency range at an input power lower than 0 dBm, according to recent reports.

Measurement results showed that the presented 37 GHz wide-band programmable divide-by-*N* FD is suitable for adoption in a 27.3 to 33 GHz PLL block of 31.3 to 45 GHz ALMA band-1 receivers or other ultra-wideband, low power applications.

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