Mian Cheng, Jin-shu Su, Jing Xu, 2017. Real-time pre-processing system with hardware accelerator for mobile core networks. *Frontiers of Information Technology & Electronic Engineering*, **18**(11): 1720-1731.
http://dx.doi.org/10.1631/FITEE.1700507

Real-time pre-processing system with hardware accelerator for mobile core networks

Key words: Mobile network; Real-time processing; Hardware acceleration

Corresponding author: Jin-shu Su
E-mail: sjs@nudt.edu.cn

ORCID: http://orcid.org/0000-0001-9273-616X

Motivation

- Effectively monitoring and processing security incidents that occur on the mobile Internet is an important challenge for network managers.
- Conventional approaches are still limited to only a few common protocols (e.g., HTTP) and cannot satisfy the requirements of mobile networks.
- With the constantly increasing of network bandwidth, high-performance real-time collection of network traffic in a limited time and without loss is still a challenge.

Main idea

- A hardware accelerator, performs processing which has a simple calculation procedure but consumes plenty of computing resources, such as packet decapsulation and character transformation of PPP frames in the CDMA2000 core network.
- Then for those operations that require significant resource overhead, such as packet decompression and recombination, we use a multi-core processor to significantly improve the processing capacity in a high-speed mobile core network.
- The implemented prototype can quickly process each encapsulated packet and effectively distribute the restored packet to back-end servers.

Method

1. The system consists of a multi-core processor, a hardware accelerator, and peripheral units such as ternary content-addressable memory (TCAM) and static random access memory(SRAM).
2. We use a FPGA to perform the packet processing acceleration, including character transformation (Algorithm 1) , packet reconstitution and packet distribution.
3. We use a XLP432 multi-core processor to achieve complicated calculation procedures, such as VJ Decompression and gateway address learning

Major results

- When using hardware accelerator, results indicate that the performance of our system improves by 27%, 57%, and 50% when dealing with three different packet types.

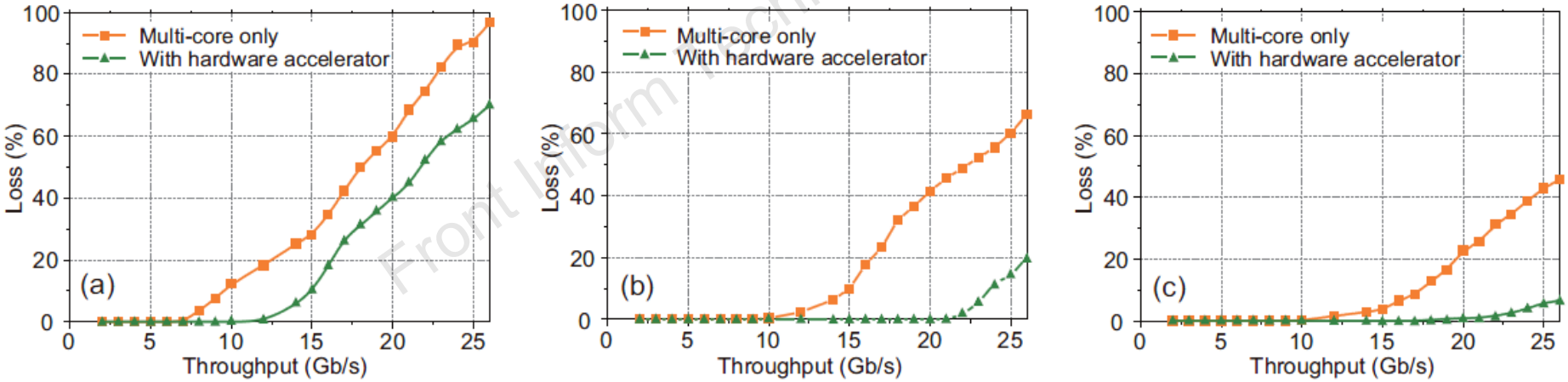

Fig. 11 Packet loss experiment on different types of packet: (a) 64-byte VJ; (b) multi-internal fragment; (c) cross fragment

Major results

- Performance evaluation of the overall system. Evaluation results showed that our system can achieve a speed of at least 18 Gb/s with no packet loss.

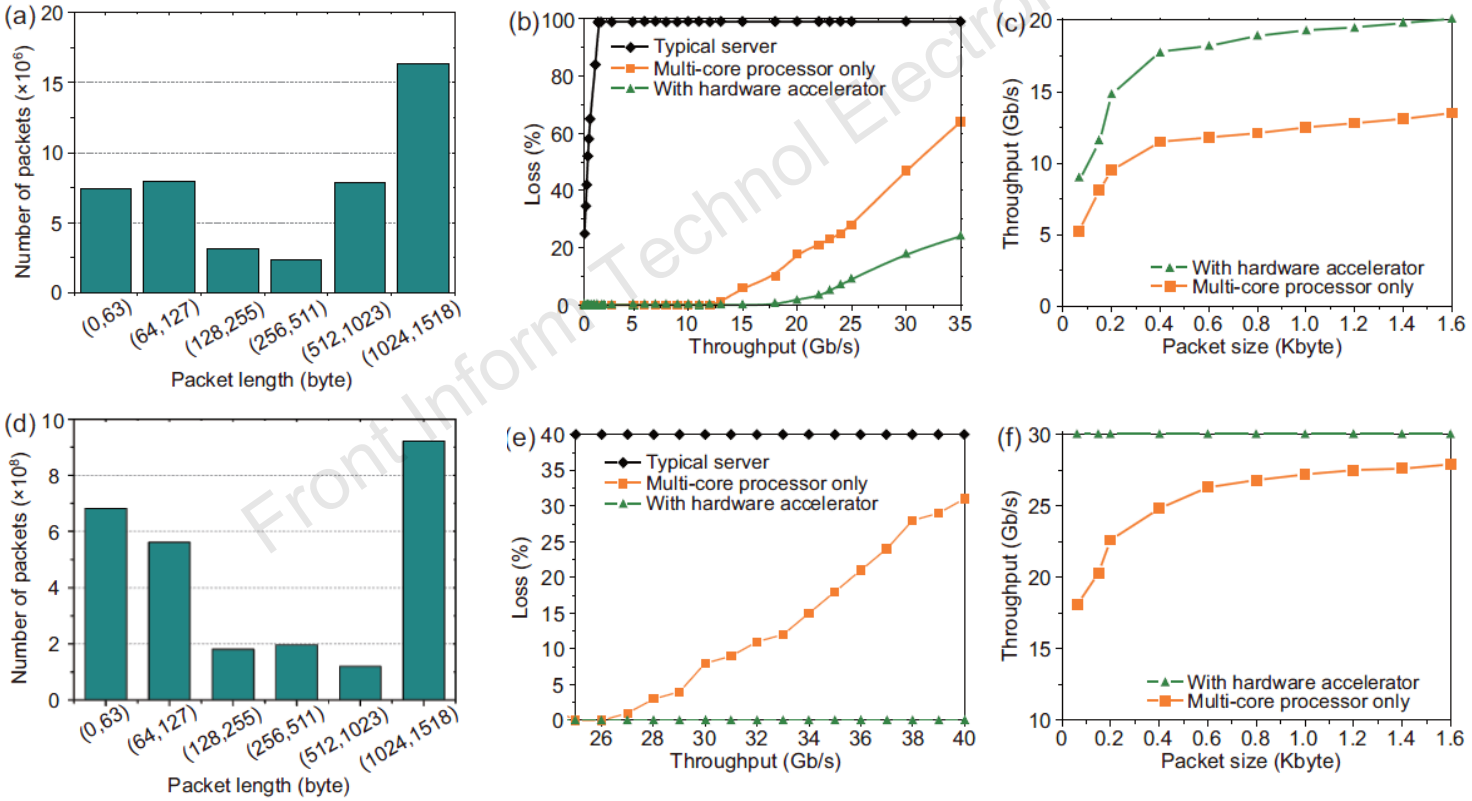

Fig. 12 Results of system performance: (a)–(c) are respectively the packet size distribution, packet loss rate, and throughput in the CDMA2000 core network; (d)–(f) are respectively the packet size distribution, packet loss rate, and throughput in the TD-SCDMA core network

Conclusions

- For reducing the processing pressure on back-end detection server, an FPGA-based hardware accelerator and a multi-core processor were implemented to handle different stages of packet processing.

- Evaluation results showed that our system can achieve a speed of at least 18 Gb/s with no packet loss.