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A 0.20–2.43 GHz fractional-*N* frequency synthesizer with optimized VCO and reduced current mismatch CP

Key words: Frequency synthesizer; Charge pump (CP); Voltage-controlled oscillator (VCO); Current mismatch; Phase noise

Corresponding author: Wei ZOU
E-mail: weizou@hust.edu.cn
ORCID: https://orcid.org/0000-0002-8683-9880

Motivation

1. Fractional-*N* phase-locked loop (PLL) based frequency synthesizers have gained popularity in multi-band wireless communication systems as local oscillators.

2. A critical challenge in PLL synthesizers is to achieve a wide output frequency range together with low spurs and low phase noise.

3. Spurs can create a reciprocal mixing problem, and poor phase noise would degrade the noise floor and the selectivity of a multi-standard reconfigurable transceiver.

Main idea

1. Voltage-controlled oscillators (VCOs) that determine the out-band phase noise of a PLL based frequency synthesizer are optimized using an automatic amplitude control technique and a high-quality factor figure-8-shaped inductor.

2. A charge pump (CP) with a mismatch suppression architecture is proposed to improve the CP current match and reduce the PLL phase errors.

Method

1. An automatic amplitude control (AAC) technique is employed in the VCO core to help sustain an optimal amplitude across the tuning band.

2. An optimized high-quality-factor figure-8-shaped inductor is used to ameliorate the phase noise and reduce magnetic coupling.

3. Two rail-to-rail operational amplifiers are used to maintain the current match as CP output voltage changes.

Major results

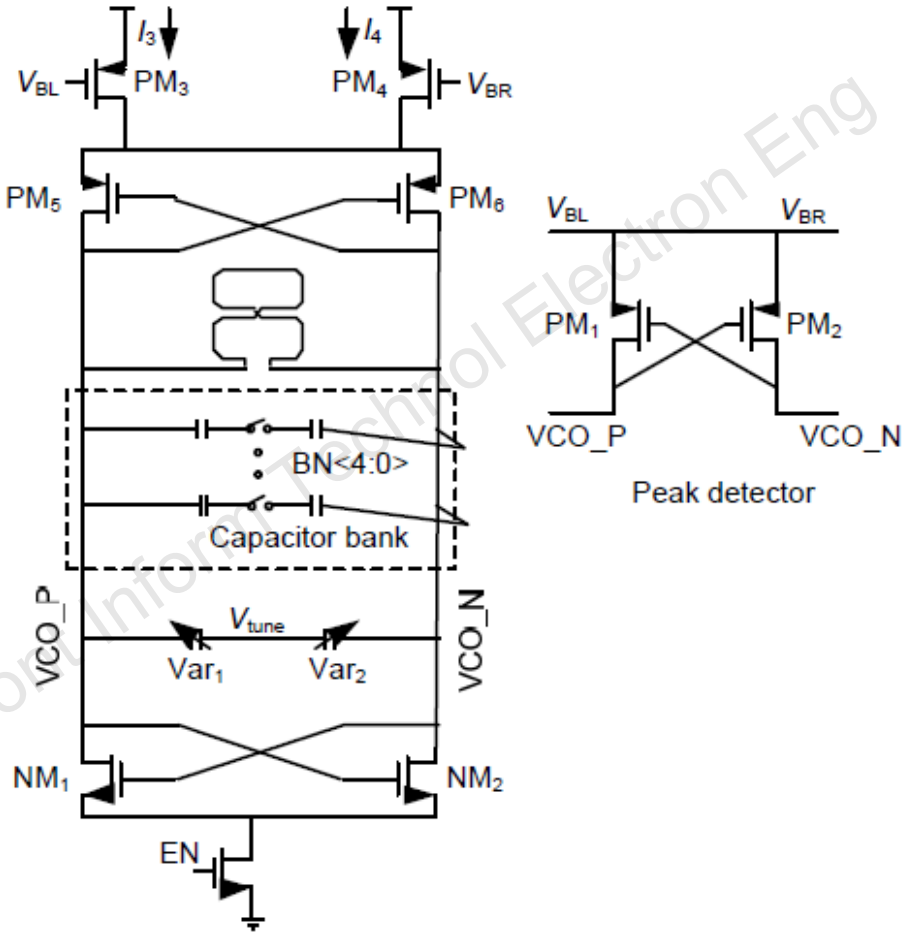

Fig. 1 The proposed voltage-controlled oscillator (VCO) with an automatic amplitude control (AAC) circuit and a figure-8-shaped inductor

Major results (Cont'd)

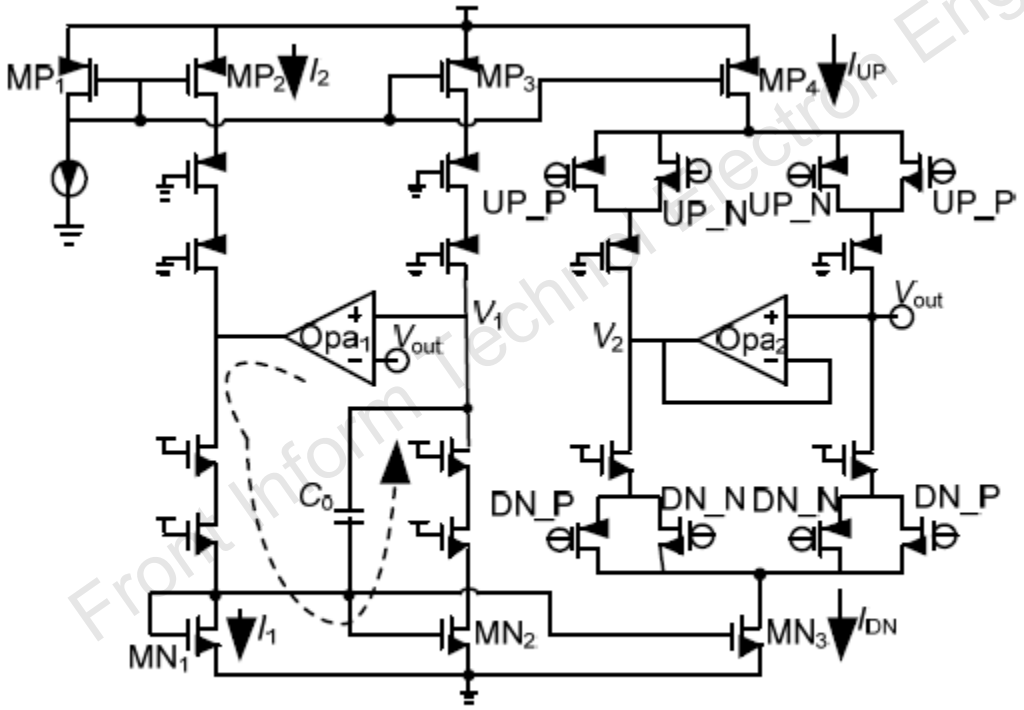

Fig. 7 The proposed CP topology

Major results (Cont'd)

Table 2 PLL performance comparison

Reference	CMOS process (nm)	Freqency tuning range (GHz)	F_{REF} (MHz)	Phase noise	Jitter (ps)	Reference spur (dBc)
Deng et al. (2014)	65	0.01–6.60	36	−135.3 dBc@3 MHz		−79
Wu et al. (2017)	40	1.73–3.38	50	−109 dBc@100 kHz	0.42	
Chang WS et al. (2014)	180	2.12–2.40	48	−134.8 dBc@10 MHz	0.26	−55
Narayanan et al. (2016)	65	4.34–4.94	40	−131.8 dBc@10 MHz	0.13	−70.8
This paper	180	0.20–2.43	24	−122.8 dBc@1 MHz	0.96	−65.3

Reference	In-band fractional spur (dBc)	Out-band fractional spur (dBc)	Power (mW)	FOM[a] (dB)	FOMT[b] (dB)
Deng et al. (2014)			16–26	177.3	−203.3
Wu et al. (2017)	−42		10.7	184.7	−200.9
Chang WS et al. (2014)	−48	−70	17.3	169.6	−171.5
Narayanan et al. (2016)	−59.2	−75	6.2	177.7	−179.9
This paper	−50	−71	27.3	176.1	−200.7

a: $\mathrm{FOM} = 10\lg\left[\left(\frac{f_0}{\Delta f}\right)^2\left(\frac{1\,\mathrm{mW}}{\mathrm{power}}\right)\right] - L(\Delta f)$; b: $\mathrm{FOMT} = L(\Delta f) - 20\lg\left(\frac{f_0}{\Delta f}\frac{\mathrm{FTR}}{10}\right) + 10\lg\left(\frac{\mathrm{power}}{1\,\mathrm{mW}}\right)$

Conclusions

1. An AAC technique and a high-quality-factor figure-8-shaped inductor have been used to improve the performance of the proposed VCO.

2. A circuit architecture that flexibly adopts two rail-to-rail operational amplifiers has been proposed to improve the CP current match and the linearity.

Xuecheng ZOU received his PhD degree in microelectronics and solid state electronics from the Department of Electronic Science and Technology, Huazhong University of Science and Technology, Wuhan, China, in 1993. He is currently a professor with the School of Optical and Electronic Information, Huazhong University of Science and Technology. His main research areas include DC-DC converter design and Internet of Things.