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Influence of polarized bias and porous silicon morphology on the electrical behavior of Au-porous silicon contacts*

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Abstract: This paper reports the surface morphology and I-V curves of porous silicon (PS) samples and related devices. The observed fabrics on the PS surface were found to affect the electrical property of PS devices. When the devices were operated under different external bias (10 V or 3 V) for 10 min, their observed obvious differences in electrical properties may be due to the different control mechanisms in the Al/PS interface and PS matrix morphology.

Key words: Porous silicon, Morphology, Electrical properties
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INTRODUCTION

Porous silicon (PS) attracts the attention of many researchers due to the possibility of developing PS based devices, including optoelectronics, photo resistors, solar cells and light emitting diodes (Balucani *et al*., 1999; Palma *et al*., 1999a; Stievenard and Deresmes, 1995). To integrate PS into electronic circuits or to develop PS based devices, the electrical properties of this material must be studied thoroughly. It is a difficult case because this material has a very irregular surface topography, which causes instabilities in PS-based devices. There are a number of hypotheses, which consider that the physical phenomena in a porous material is responsible for the magnitude and nature of the conductivity in PS. Chorin *et al*.(1994) commented that chemical environment affected the electrical conductivity of PS. Stievenard and Deresmes (1995) reported that the conductivity was governed by the width of the channel resulted from the partial depletion of silicon located between two pores. The depleted region was due to the charges trapped on surface states associated with the Si-SiO_2 interface where SiO_2 was the native silicon oxide. Averkiev *et al*.(2002) indicated that the localized states with energy distribution near the conduction and valence band edges controlled the carrier transport. Two researcher groups (Zimin and Bragin, 1999; Balagurov *et al*., 2000) proposed that the role of hydrogen on the electrical properties of PS depended on the porosity, morphology of voids and the type of doped impurity in the original silicon substrate.

The effect of temperature on the current density-voltage (I-V) characteristic of metal contacts on PS films was observed in experiments (Pazebutas *et al*., 1995; Chen *et al*., 1994a; 1994b; Remaki *et al*., 2003; Aroutiounian and Ghulinyan, 2003; Balagurov *et al*., 2001). Those authors proposed different mechanisms. Some of the authors assumed that

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thermo-ionic emission or diffusion over barrier controlled the current densities of the devices, but the other authors proposed that tunneling mechanism or electric field dependence of PS conductivity as a dominant mechanism. Deresmes *et al*.(1995) considered the conduction is limited by a surface mechanism associated with hopping of carriers from site to site, each site corresponding to a dangling bond. Ciurea *et al*.(1998) proposed the quantum confinement model to explain the electrical transport properties of PS film.

An energy band diagram around the interface between PS and bulk Si was also used to analyze PS device (Palma *et al*., 1999b; Kaganovich *et al*., 1999; Dafinei and Dafinei, 1999; Cadet *et al*., 1994; Romstad and Veje, 1997). It was supposed that PS has a band gap of about 1.8 eV. Furthermore, the interface of PS and bulk Si with band gap of about 1.1 eV, has been postulated with band discontinuities occurring at both valence and conductions bands. The interface of PS and top metal contact has been shown with slight band bending.

Up to date, there are few reports of work on the influence of bias on the electrical properties of PS based devices. In this paper, we report the I-V characteristics of PS based devices operated under an external polarized bias for 10 min. The surface morphology of PS was studied by scanning electron microscopy (SEM). Furthermore, infrared (IR) spectrometry showed the passivation of PS surface by oxygen, carbon and hydrogen atoms.

EXPERIMENTS

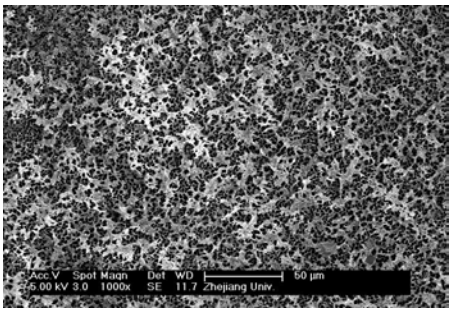
PS layers were prepared on (100) P-type wafers of crystalline Si with resistivity of 1~10 Ω·cm. To improve the homogeneity of PS films, Al ohmic electrodes were prepared by thermal evaporation on the backside of the wafers electrochemically etched in a HF-C_2H_5OH electrolyte (with volume ratio of 1:2) using a constant current density of 30 mA/cm^2. The etching time was varied from 30 min to 90 min. A 50 W light was used as back illumination during etching. After etching, the backside Al film was removed with aqueous HF. Then, the samples were washed in deionized water and dried in air. The Au films were deposited by vacuum sputtering on both sides of the wafers.

Their I-V characteristics, Fourier transform infrared (FTIR) spectroscopy, Raman spectroscopy and scanning electron microscopy (SEM) were used to study the samples. The infrared absorption spectra were taken using a Bruker IFS 66v/S FTIR spectroscope. The observations of the samples' appearance were carried out using a FEI SIRION FESEM. Raman spectra excited with 532 nm line were measured using a Nicolet Almege Raman Spectrometer. I-V measurements of the sandwich configuration, Au/PS/c-Si /Au, were taken using a computer-interfaced KEITHLEY 4200 semiconductor characteristics system. All the measurements were carried out at room temperature.

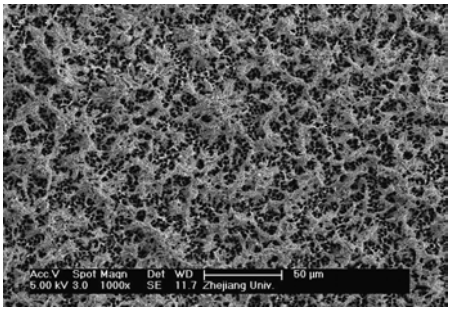
RESULTS AND DISCUSSION

Fig.1 shows the surface morphology of the PS etched at different time. These images show that the PS has an alveolar columnar structure. The columnar pores are not regular and as they have 3~5 μm diameter, they are called macro pores from here on. Usually, the silicon optical phonon line shifts to lower frequency and broadens asymmetrically with decreasing nano crystal size (Boukherroub *et al*., 2002). In our experiments, the Raman spectrum of PS was almost identical in the PS etched at different time, as shown in Fig.2. A sharp peak at 521 cm^{-1} is apparent, meaning the lack of quantum confined effect in our PS samples.

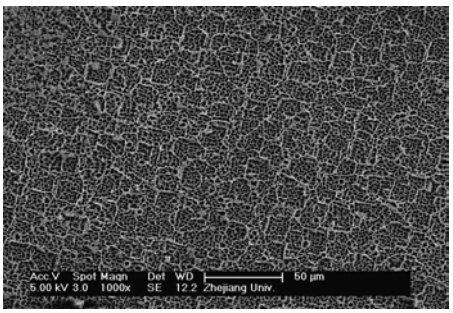
Furthermore, the PS surface was almost smooth and flat. Many fabrics were observed on the surface of the PS etched for longer than 60 min, as shown in Fig.1a and Fig.1b, which is due to the stain reaction between Si and HF acid. During anodic etching, the material between pores was generally depleted of carriers, and the presence of a depletion layer is responsible for current localization at pore tips. After reaching to a critical thickness, pore walls are devoid of holes and hence inert to lateral anodic etching (Koker *et al*., 2003). But chemical etching is always proceeding during anodic etching. During the stain etching process, the etching rate of the Si (111) crystal plane is about two orders of magnitude larger than that of the (100) and (110) crystal planes, so the PS can be tailored to form slice-like structure, as shown



(a)



(b)



(c)

Fig.1 SEM images of the as-prepared PS etched for different time (a) 90 min; (b) 60 min; (c) 30 min

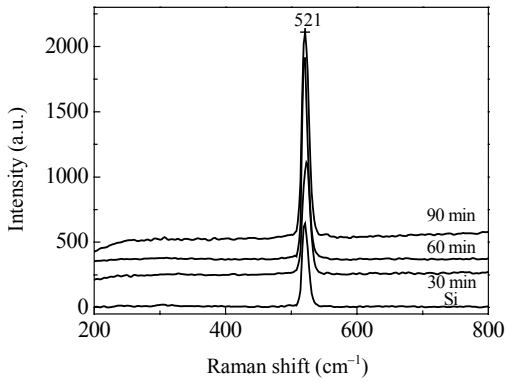


Fig.2 Raman spectra of the PS samples etched for different time, as illuminated in image

in Fig.1c. They were lying down due to collapse caused by the wallop of the H_2 bubbles produced by electrochemically-etched process. The EDS (energy-dispersive spectroscopy) image shows that the substance on the PS surface consists of silicon and oxygen.

Fig.3 shows the IR absorption spectrum of the PS etched at different time under different external bias. The PS samples show Si-O-Si absorption peaks

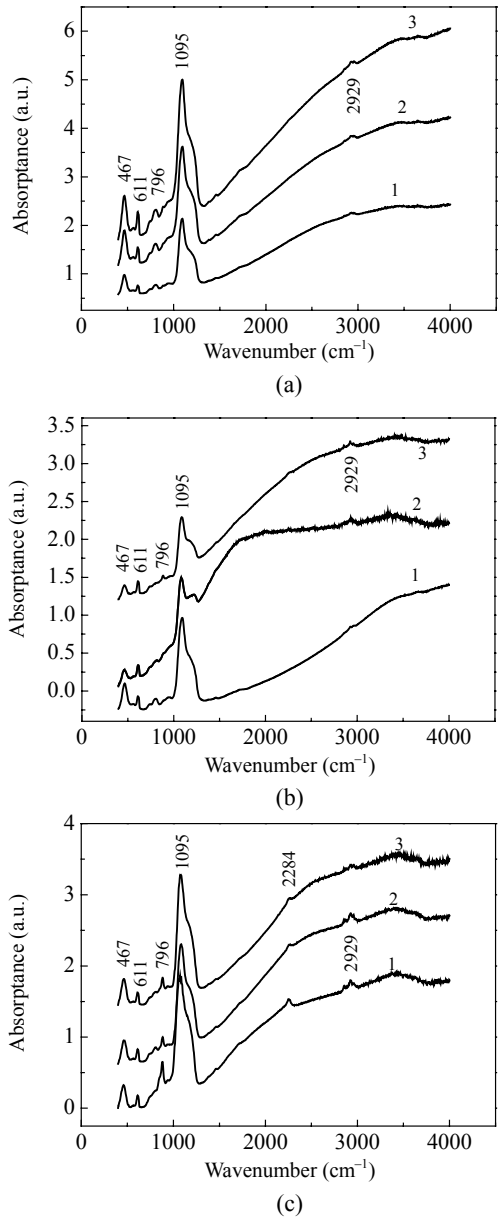


Fig.3 FTIR spectra of the PS devices operated under (a) 10 V; (b) 3 V and (c) 0 V external bias. Curves 1, 2 and 3 are for PS samples etched for 90, 60 and 30 min, respectively

at 467, 796 and 1095 cm^{-1} and the C-H stretching modes at around 2929 cm^{-1} (Li *et al*., 2000). The absorption peak at 611 cm^{-1} is due to the Si-Si bonds vibration. It can be seen that the intensity of the Si-O-Si absorption peak at 1095 cm^{-1} decreases continuously with increasing etching time, as shown in Fig.3a, while external forward bias was 10 V. On the contrary, the intensity increases with increasing etching time, while external forward bias was 3 V (Fig.3b). But, the intensity in all samples without external bias was the same with increasing etching time, as shown in Fig.3c.

I-V characteristics corresponding to the different external bias applied in Au/PS/c-Si/Au structures were measured in the –10 V to 10 V range. Fig.4 shows the I-V curves of the PS device without external bias and with 3 V, 10 V external bias for 10 min. The structure of the device is also shown in the inserted image of Fig.4. The PS samples used in these devices were etched in 60 min. When the device was operated with 10 V external bias for 10 min, variation of the current by a factor about 30% was observed compared with that of the device without external bias. But the forward current shows a 90% decrease when the devices were operated under 3 V external bias for 10 min, as shown in Fig.4. The difference between the two devices may be associated with the gradual oxidation of the porous silicon skeleton under operation in the atmosphere for different polarized bias and the controlled mechanism of conduction in different PS devices.

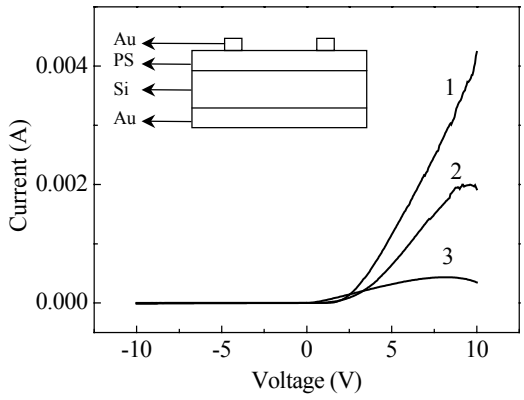


Fig.4 I-V curves of PS samples operated under different external bias. Curves 1, 2, 3 are for PS samples operated 0 V, 3 V and 10 V external bias. The inserted image shows the structure of the PS device

The PS samples etched for different time exhibit distinct difference of the forward current when these devices were operated under different external bias, as Fig.5 shows. When the devices were operated under 3 V external bias for 10 min, the current of the sample etched in 30 min shows small decrease of the current compared with that of the samples etched for 60 min or 90 min. The current variation of the sample etched for 30 min was large, but the current variation of the others devices showed small change of the forward current when the devices were operated under 10 V external bias for 10 min.

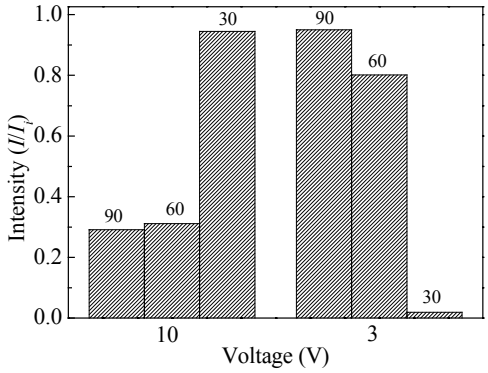


Fig.5 Columnar representations of the PS device's different forward current under different external bias. The numbers 90, 60 and 30 represent the etching time of the samples. The reference current (I_i) is the device's forward current with 0 V-applied bias

Although many reports on the electrical properties of PS have been published, the mechanism governing the current transport process through PS structures is still not clear. Some authors considered that the presence of a large concentration of interface states controlled the current of the devices (Palma *et al*., 1999b). But the others thought that the metal-porous silicon barrier played a significant role in the transport mechanisms (Diligenti *et al*., 1996). Furthermore, the model based on passivation of hydrogen was also proposed (Zimin and Bragin, 1999). In addition, it was indicated that the total current of devices was governed by carrier transport in the high resistivity PS layers (Peng *et al*., 1996). In our experiment, when the devices were operated under 3 V external bias, the total current of the device was dominated by carrier transport at the Al/PS interface. The SEM images showed that the sample etched for

longer time has many slices on the surface (Fig.1a). As the external voltage on this surface layer drops during operation, the increasing temperature of the devices causes oxidation of the PS surface and then the resistivity of the surface layer increases, which leads to decreasing the forward current of the device. Furthermore, the intensity of Si-O-Si bonds vibration increases with the increase of the surface slices, as shown in Fig.3b. But in high external bias (10 V), the potential barrier in the Al/PS interface breaks down, so the PS layer voltage drops. The total current of the device is controlled by the carrier transport in the high resistivity PS layer, which also can be explained by the results of surface observation and element analysis. When the device is operated under high external bias (10 V), the voltage on the PS layer drops, and the total current is controlled by the current flow through the PS layer. When the sample was etched for shorter time, resulting in the large internal surface of the pores, the oxidation is severe under a high bias, leading to the decrease of the device's forward current, as shown in Fig.4. For applied bias of 3 V to 10 V, the controlling mechanism of the electrical behavior may be related to the combined contribution of the PS layer and the surface layer. In some locations, the potential barrier in the Al/PS interface breaks down, so the voltage in the PS layer drops. But in other locations, the total current of the device was controlled by carrier transport at the Al/PS interface. The further study is necessary to exploit the real mechanism.

CONCLUSION

In this paper, the surface morphology and the I-V curves of the PS samples etched for different time were investigated. The fabrics observed on the surface of the PS affected the electrical properties of the PS devices. When the devices were operated under different external bias (10 V or 3 V), the observed obvious difference of electrical properties was due to the different mechanism. While the device was operated at low external bias, the states of the Al/PS interface might control the device's current, although the high resistance PS layer can also control it.

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