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Test access to deeply embedded analog terminals within an A/MS SoC

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Abstract: This paper presents a standard scalable and reconfigurable design for testability (SR DfT) in order to increase accessibility to deeply embedded A/MS cores and to limit application of costly off-chip mixed-signal testers. SR DfT is an oscillation-based wrapper compatible with digital embedded core-based SoC test methodologies. The impact of the optimized oscillation-based wrapper design on MS SoC testing is evaluated in two directions: area and test time. Experimental results are presented for several SoCs from the ITC'02 test benchmarks with inclusion of eight analog filters.

Key words: Scalable design for testability (DfT), Reconfigurable architecture, Embedded A/MS testing, Modular testing, Built-in self test (BIST)

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INTRODUCTION

Mixed-signal SoCs, including analog, mixed-signal and digital circuits, have recently received much attention particularly in communications and multimedia applications. The limited numbers of SoC test nodes lead to a highly structured DfT (design for testability) methodology for accessibility to the individual embedded cores. The DfT-based methodologies support designers to solve the test access challenges. These DfT methodologies are more feasible for digital SoCs than mixed-signal SoCs.

This paper presents a scalable and reconfigurable DfT to extend core-based test architectures to support deeply embedded analog terminals within an A/MS SoC. It also presents necessary test access mechanism and test scheduling algorithm for this architecture. The experimental results for several SoC's from ITC'02 benchmarks (Marinissen *et al*., 2002) augmented with eight filters show the cost effectiveness of this approach.

This paper is organized as follows. Section 2 gives a brief overview on test accessibility and related research. Section 3 shows our contribution and test hardware block diagram. Section 4 is an oscillation-based built-in self test (BIST) overview. Section 5 introduces scalable and reconfigurable (SR) DfT design and test strategy. The SR DfT initialization is presented in Section 6. Section 7 introduces the test access strategies in our approach. Test scheduling algorithm is presented in Section 8. Experimental results are reported in Section 9, and the conclusion of this paper is given in Section 10.

TEST ACCESSIBILITY RELATED RESEARCH

The accessibility to the embedded blocks in the whole complex SoC chip is a basic challenge. To simplify the test access and the test application, one of the first proposed approaches has been the macro test technique (Beenker *et al*., 1990). In macro testing, the first step consists of partitioning the design into independently testable macros. The second step consists of developing a suitable test method for each macro and defining an embedded test pattern gen-

erator. Finally it is required to produce a test plan for the whole circuit. The transformation of a test protocol defined at a lower-level macro into a test protocol defined at a higher-level macro is done by a test protocol expansion (Marinissen *et al*., 1993).

Nowadays the core-based test technique has replaced the macro test technique. Core-based testing needs an infrastructure to simplify the test application and to meet requirements between core provider and core user. A scalable mechanism for test access to embedded reusable digital cores is presented in (Marinissen *et al*., 1998). The mechanism has a wrapper to isolate an IP core from its environment during test time, and also presents a test data transport mechanism. The extension of this architecture to mixed-signal circuits has been presented in (Seuren and Waayers, 2004), but it does not explicitly specify the testing of the analog modules. In this method, test data generation and test result analysis for analog terminals are performed off chip.

Zorian *et al*.(1998) introduced a conceptual test access architecture that enables modular test development. In this approach an embedded core has been isolated from its surrounding circuitry and electrical test access has been provided for the core. This approach finally led to IEEE 1500 standard (IEEE Computer Society, 2005), which is a testability method for embedded core-based integrated circuits. This standard is independent of the underlying functionality of the integrated circuit, and has also a user defined test access mechanism.

Various test access mechanism (TAM) architectures can be found in literature for embedded cores in a digital SoC. Three scan-based test architectures are described in (Aerts and Marinissen, 1998): multiplexing architecture, distribution architecture, and daisy-chain architecture. In the multiplexing architecture, all modules get access to the full available SoC TAM width. Since only one module can be accessed at a time, interconnect testing between modules is cumbersome. In the distribution architecture, the total available SoC TAM width is distributed over the wrapped modules. In the daisy-chain architecture, all modules have access to the full available SoC TAM width. Due to the bypass mechanism for each embedded module, any subset of wrappers can be accessed simultaneously. Each bypassed module adds a time slot per test pattern to the module under test. This leads to the conclusion that in this architecture time is wasted propagating through bypass flip-flops. In (Waayers *et al*., 2005) a definition of daisy-chain architecture reducing the time wasted in embedded digital cores has been presented.

The use of BIST for high volume production of mixed-signal ICs can overcome the accessibility challenge and reduce the cost per chip during production-time testing. The BIST approaches and the use of existing resources to generate a cost-effective test planning for the functionality testing of A/MS cores have been presented in (Lubaszewski *et al*., 1996; 1997; Renovell *et al*., 1996; 1997; Cota *et al*., 2000). Another approach is the addition of on-chip data converters for testing analog cores. These data converters eliminate the demands of high-end mixed-signal test equipment (Sehgal *et al*., 2003; 2005).

In oscillation-based BIST methodology, the circuit under test is converted to an oscillator in the test mode and the oscillation frequency which is closely related to the behavior and performance of the circuit under normal operation is measured (Arabi and Kaminska, 1997a; 1997b; 1999). Using digital signals coming from a ΣΔ modulator and a level crossing detector, the amplitude of the oscillation signal has been measured and the fault coverage has been improved (Vazquez *et al*., 2002; Huertas *et al*., 2002b).

An oscillation-based analyzer suitable for modular testing requirements has been presented in (Niaraki *et al*., 2006; 2007). This analyzer measures the frequency and amplitude of oscillation signal and makes necessary decisions to control the measuring process.

In the work presented here, we have developed an oscillation BIST analyzer as a deep analog test wrapper in a mixed signal SoC. The deep analog test wrapper is compatible with IEEE 1500 test wrapper and allows the analog and digital cores to be tested concurrently in a unified test strategy which results in test time reduction. Sharing deep analog test wrapper for the time multiplexed utilization of analog cores decreases the needed hardware overhead in this method. We have considered three SoCs from ITC'02 test benchmarks that have been included with eight filters. We demonstrate the simulation results for simultaneously using the deep analog test wrapper

and IEEE 1500 embedded core-based wrapper for these mixed-signal SoCs.

CONTRIBUTION AND OVERVIEW OF PROPOSED TEST HARDWARE

The IEEE 1500 standard presents a testability method for embedded digital cores within a SoC. Test stimuli are delivered to the embedded digital core and test responses are collected through an improved accessibility (IEEE Computer Society, 2005). Boundary-scan architecture, IEEE 1149.1, transfers digital data to the boundary of the SoC (IEEE Computer Society, 1990). These methods forego addressing analog circuits and focus on facilitating efficient test of digital aspects of SoCs. Analog test bus standard for analog/mixed-signal chips, IEEE 1149.4, extends the boundary scan architecture by addition of the analog and parametric measurement capabilities for the analog signals that exist in the boundary of a chip (IEEE Computer Society, 1999).

On the other hand, Philips in (Seuren and Waayers, 2004) has presented mixed-signal DfT architecture to support digital terminals of the mixed-signal embedded cores. In Philips approach, it is supposed that the analog signals to be measured are already at the chip level pins. As the complexity of mixed-signal SoCs increases, there is a further need to test deeply embedded analog cores as well.

This paper presents a scalable and reconfigurable DfT that works based on oscillation BIST analysis and extends core-based test architectures to support deeply embedded analog cores within a SoC. Fig.1 shows our test hardware block diagram. To test the deep analog terminals of A/MS cores, we encounter two problems: test evaluation problem and test access problem. We design an oscillation-based wrapper including oscillation-based analyzer and compatible with the digital core-based SoC test architecture. We refer to our wrapper design as SR DfT, which is responsible for test evaluation and has been initialized through an optimized test access mechanism.

As shown in Fig.1, two test access mechanisms compatible with core based test architecture would be considered: test access for inside the wrapper and test access between the wrappers.

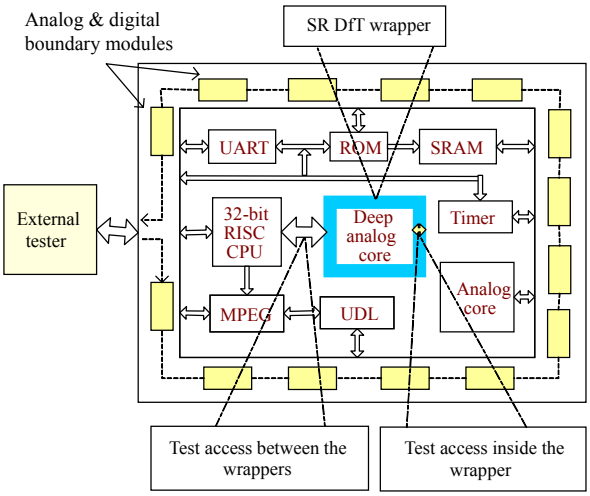


Fig.1 Test hardware block diagram including SR DfT and two test access mechanisms compatible with core based test architecture

OSCILLATION-BASED BIST OVERVIEW

Fig.2 shows the block diagram for a system modified to apply oscillation-based BIST and connected to a level crossing detector and a ΣΔ modulator for on chip evaluation. Fig.3a shows the oscillation signal of a high-pass filter. The filter is a biquadratic filter existed in a dual tone multifrequency receiver with the oscillation frequency of 2010 Hz and the amplitude of 3.86 V. Figs.3b and 3c show the outputs of the level crossing detector and the ΣΔ modulator.

To extract the oscillation-based parameters from these outputs, let $x(t)$ be a sinusoidal oscillation signal of period T, amplitude A and DC-level B. This signal can be approximated by:

$$x(t)\approx B+A\sin(\omega t+\varphi), \tag{1}$$

where $\omega=2\pi/T$ and φ represents the phase-shift.

The characteristic parameters of such a signal are as follows (Vazquez *et al*., 2002):

$$Amp\approx(2A/\pi)N\pm2, \tag{2}$$

$$f\approx T_{osc}/T_s\pm1, \tag{3}$$

where $N=T_{osc}/T_s$ is the oversampling ratio.

The measurement accuracy is mainly determined by the oversampling ratio and the quantization error, which includes the phase shift φ effects and introduces the bounded terms (±2, ±1) (Vazquez *et al*., 2002).

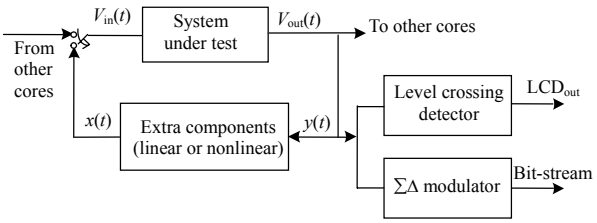


Fig.2 Testable circuit connected to a level crossing detector and a ΣΔ modulator

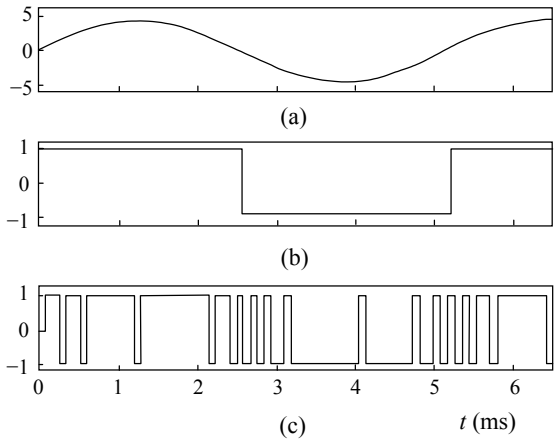


Fig.3 (a) Oscillation signal; (b) Level crossing detector output; (c) ΣΔ modulator output of a high-pass filter (unit: volt)

SR DfT FOR DEEP ANALOG TERMINALS

The SR DfT wrapper connects a standard core-based architecture to an embedded A/MS core supported by oscillation-based BIST. The SoC wrapper control interface sends control signals to initialization of the SR DfT wrapper as well as the 1500 and JTAG wrappers.

Fig.4 shows the structure of SR DfT. It is made up of wrapper controller and the wrapper circuitry. It also includes a bypass register and two multiplexers. The multiplexers are selected between the controller registers, the bypass register or the data registers of the analog test circuitry.

The purpose of the SR DfT wrapper is as follows:

(1) It is a fully digital testable infrastructure;

(2) Its associated test strategy is fully compatible with the digital core-based test strategies like IEEE 1500 standard;

(3) It enables reuse of existing test hardware and test programs;

(4) It enables verification of the test strategy at the chip level;

(5) Different A/MS cores, supported by oscillation-based BIST, can be concurrently tested by their own SR DfTs;

(6) Using an oscillation-based test methodology, test stimuli are internally generated and test responses are internally analyzed;

(7) It reduces the requirements for a sophisticated test access mechanism.

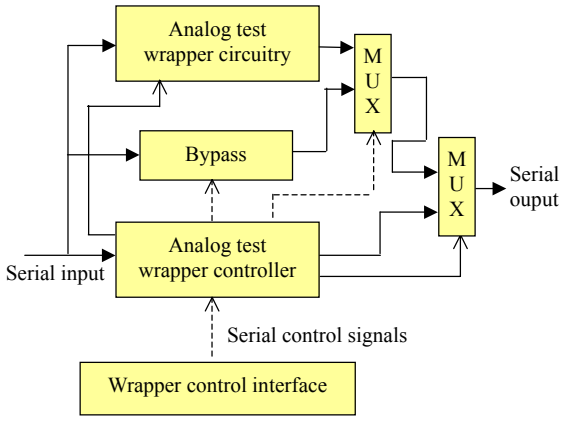


Fig.4 The structure of SR DfT

SR DfT design

SR DfT consists of two basic units: the wrapper controller and the wrapper circuitry. Fig.5 shows its controller. It is a state machine including a shift register, an updating register to prevent random perturbation on control signals, and a decoding logic. The controller states control the test evaluation steps.

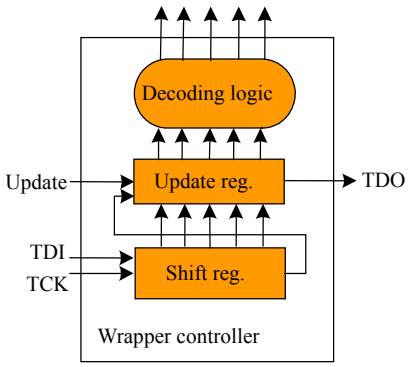


Fig.5 The SR DfT wrapper controller

Fig.6 shows the wrapper circuitry including a logic unit and a register unit. The logic unit controls the frequency and the amplitude measurement process of the oscillation-based technique. The register unit contains two types of registers: those not modified during the test process are called 'constant registers', and the rest are called 'variable registers'. A constant register gets its initial value from the TDI port controlled by the wrapper control interface. To minimize the initialization time, a multiplexer bypasses the variable registers. Variable registers are obviously modified during the test process and controlled by the wrapper controller.

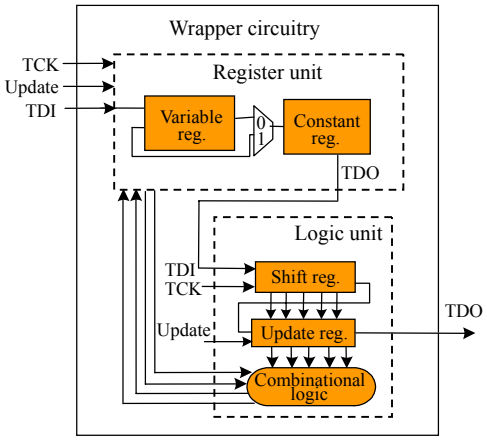


Fig.6 The SR DfT wrapper circuitry including register unit and logic unit

Fig.7 shows the complete block diagram of SR DfT. The counting process logic measures the frequency and amplitude of the oscillation signal in the separate states of the controller. The comparator compares measured values with nominal acceptable range of the frequency and amplitude values in the evaluation states. After comparison, the result of test is shown on the test result output.

The controller controls the entire test process through a sequence of states. Fig.8 shows a sequence of the controller states and inputs. The first state is the initialization state. Some A/MS cores such as an active low-pass filter require proper initial values for a safe and short transient start-up (Vazquez *et al*., 2002).

In the initialization state, the circuit is set to such a state. The initial value depends on the specification of the A/MS core under test. In the start_up state, the

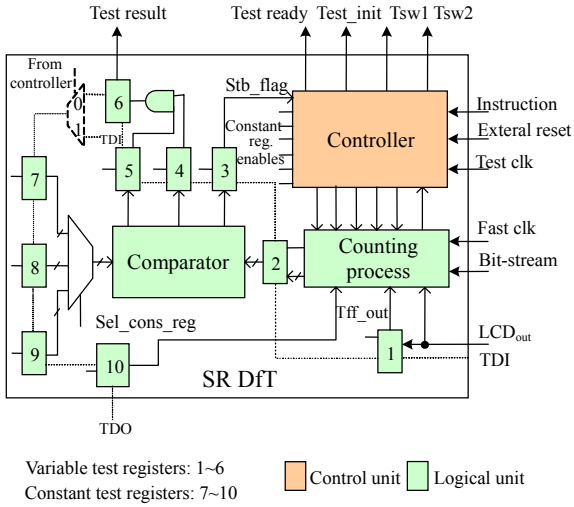
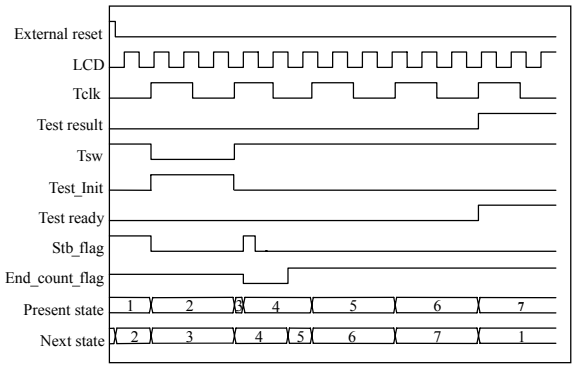


Fig.7 The SR DfT design. The nominal values are propagated through the test data path from TDI to TDO shown with dotted lines



1: reset; 2: initialization; 3: start_up; 4: count_fosc;
5: start_evaluation; 6: end_evaluation; 7: announcement

Fig.8 The sequence of the controller states

embedded core is converted to an oscillator by closing the test switches. In this step, according to the instructions of the controller, the frequency or amplitude of the oscillation signal is measured. In the next states, start_evaluation and end_evaluation, the comparator compares the measured parameter with the minimum nominal value and the maximum nominal value of the specified parameter which have been stored in the constant registers. In the announcement state, the pass/fail test result is provided on the SR DfT output.

Fig.9 shows the counting process logic in detail. This unit has two flags that handle the time control of the counting process: Stb_flag and End_count_flag. Stb_flag announces the end of the stabilization time to

the controller. The stabilization time is measured by the counting process logic and compared with the time constant register. End_count_flag is the output of the logic circuit enclosed in the dotted box as shown in Fig.9. The End_count_flag indicates the end of the counting process. The output of the shadow register stores the result of the counting process.

SR DfT test strategy

The SR DfT wrapper is responsible for generating all internal control signals to convert the circuit into an oscillator and evaluating test responses.

The first step of the SR DfT test strategy, like any other embedded digital core, consists of testing the SR DfT itself. The wrapper control interface applies the necessary serial control signals to test the wrapper.

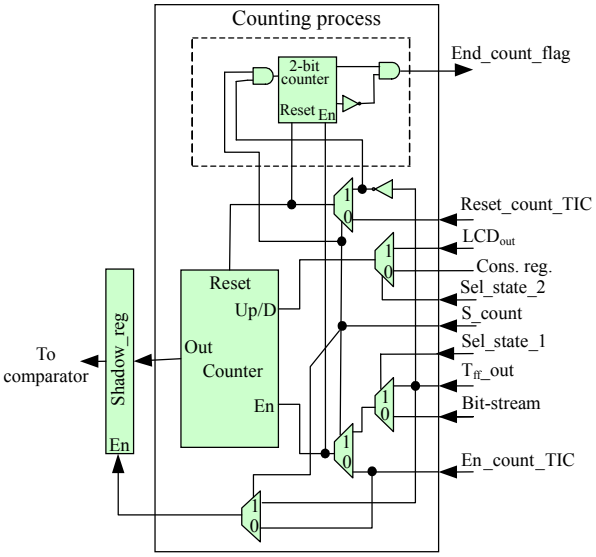


Fig.9 The counting process logic to measure the frequency and amplitude of the oscillation signal

The second step consists of initializing the constant registers and loading the controller instructions. The controller is then ready to perform the testing of the embedded A/MS core and provide the test results.

INITIALIZATION

In this section, we present the calculation of the initialization values for SR DfT. Our test example is a dual-tone multifrequency (DTMF) receiver consisting of eight different biquadratic filters. Fig.10 shows a DTMF receiver with a sequential test structure. In test mode all biquadatic filters in the feedback loop, except the filter under test, are converted to buffers using the switchable opamps (sw-opamps). This structure has been presented in (Huertas *et al*., 2002b) and guarantees a reasonable circuit performance in the application and test mode.

The linearized model of the eight filters and their maximum parameter deviation for 0.2 mismatches in capacitor ratios and process parameter variations are shown in Table 1 (Huertas *et al*., 2002a).

There are two important factors to evaluate the minimum and maximum values of the oscillation frequency and magnitude: the accuracy of the measurements and the deviation of the parameters.

We express the acceptable regions for the oscillation amplitude and frequency as follows:

$$A_{\mathrm{osc,min}}=A_{\mathrm{osc}}-\Delta A/100-2, \tag{4}$$

$$A_{\mathrm{osc,max}}=A_{\mathrm{osc}}+\Delta A/100+2, \tag{5}$$

$$f_{\mathrm{osc,min}}=f_{\mathrm{osc}}-\Delta f/100-1, \tag{6}$$

$$f_{\mathrm{osc,max}}=f_{\mathrm{osc}}+\Delta f/100+1, \tag{7}$$

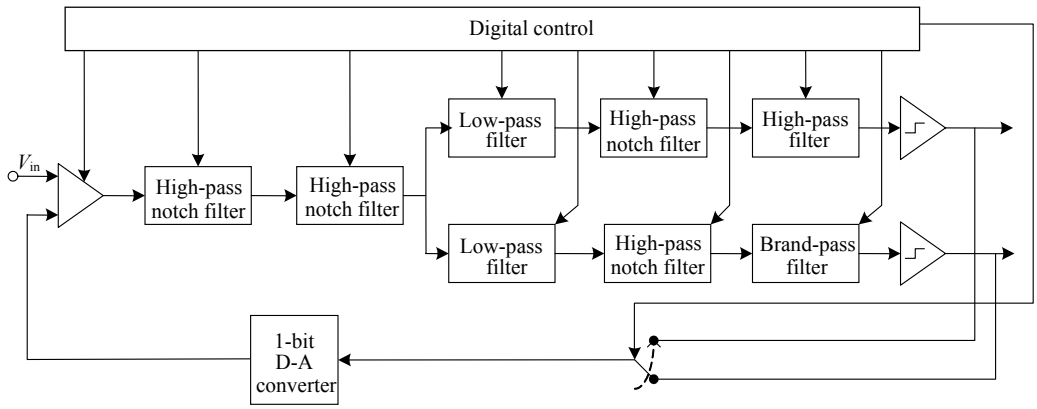


Fig.10 A dual-tone multifrequency (DTMF) receiver with a sequential test structure

Table 1 Oscillation frequency, amplitude and maximum parameter deviation for 0.2 mismatch in capacitor ratios and process parameter variations (Huertas *et al.*, 2002a)

Filter No.	Filter type	A (V_p)	f_{osc} (Hz)	ΔA (V_p)	Δf_{osc} (Hz)
1	High-pass notch	1.66	612	4.7	2.5
2	Band pass	**4.14**	602	1.9	0.9
3	High pass	0.77	751	3.9	0.8
4	Low pass	1.26	828	2.2	1.1
5	Low-pass notch	1.78	963	4.3	0.7
6	High-pass notch	1.57	1172	1.7	0.8
7	Low pass	1.24	1307	3.4	0.9
8	High pass	3.86	**2016**	4.4	1.2

where ΔA is the deviation of the oscillation amplitude and Δf is the deviation of the oscillation frequency.

For initialization, since the eighth filter has the highest oscillation frequency, this frequency is taken as the measuring frequency for all cores. Likewise, oscillation amplitude of the second filter is taken as the maximum amplitude. The maximum amplitude is used for normalizing all other core amplitudes. This is done to increase the accuracy of measuring the amplitude.

For 10% accuracy, we set the oversampling ratio of 60 for the eighth filter. Table 2 shows the oversampling ratio and the obtained acceptable regions for the eight filters.

Table 2 The setup of oversampling ratio and acceptable regions for the eight filters

Filter No.	Oversampling ratio	Amplitude counting region	Frequency counting region
1	197.6	[46,54]	[191,203]
2	200.9	[123,132]	[198,203]
3	161.0	[16,21]	[158,163]
4	146.0	[25,30]	[143,148]
5	125.6	[30,35]	[123,127]
6	103.2	[22,27]	[101,104]
7	92.5	[15,20]	[90,94]
8	60.0	[32,39]	[58,62]

TEST ACCESS STRATEGIES

For accessibility to analog terminals of embedded A/MS cores, two types of test access mechanism would be considered as shown in Fig.1. One is test access mechanism for accessing to internal scan chains of SR DfT and another is test access mechanism to connect the wrappers in a SoC.

As shown in Fig.11, we distribute scan chain flip-flops f_i into N_i groups. Where N_i is the number of pins available for scan test at SoC level divided by two and f_i is the number of scanable flip-flops. Each balanced group is bypassed with an internal bypass control pin controlled by the wrapper controller. Fig.12 shows the wrapper connections in the mixed-signal SoC. It has daisy chain architecture. In the mixed-signal SoC, all wrappers are controlled by the SoC wrapper controller.

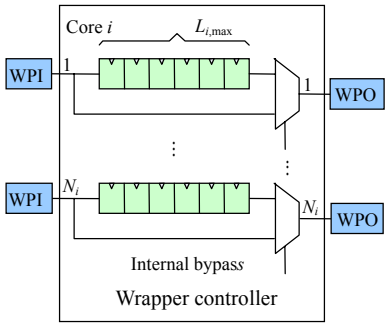


Fig.11 Test access implementation

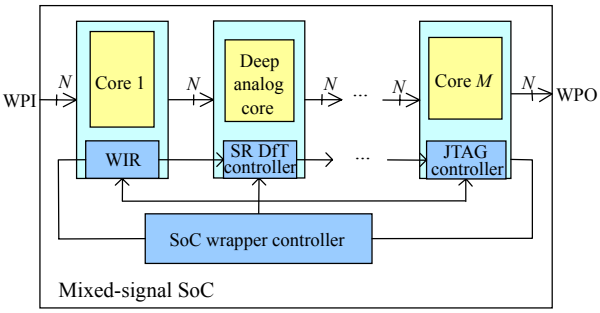


Fig.12 Daisy chain architecture for wrapper connections in the mixed-signal SoCs

For the test time analysis we use the following notations: C is defined as the set of wrapped modules embedded in a SoC and M is the number of members of C. We consider the number of test patterns P_i and the test time T_i for each module $i \in C$. T_i is the sum of shift-in time, normal mode execution time, and shift-out time for all patterns. Since the shift-in and shift-out operations can be combined for all patterns except one (first shift-in/last shift-out operation), the test time of module i can be defined as:

$$T_i=(P_i+1)f_i/N_i+P_i. \quad (8)$$

To access module i, M–1 modules each with two wrapper boundary cells (WPI and WPO as shown in Fig.11) have to be bypassed.

$$T_{\text{access},i}=2(M-1)(P_i+1). \quad (9)$$

So the total SoC time T, i.e. the sum of T_i and $T_{\text{access},i}$, is obtained from

$$T=\sum_{i=1}^{M}[(P_i+1)(f_i/N+2M-2)+P_i]. \quad (10)$$

TEST SCHEDULING ALGORITHM

We propose an effective sequential test scheduling for the whole A/MS SoC. The A/MS SoC wrapper controller sends the necessary control signals to the deep analog test wrapper and M–1 IEEE 1500 wrappers.

The proposed test scheduling algorithm is shown in Fig.13. At the first step, the SR DfT wrapper is set to Internal_Test_Mode. After internal testing of SR DfT and adjusting the initial values of constant registers, the wrapper sets to Start_Measure_Mode. At this time other digital wrappers are set to InTest_Mode and so the process of test parameter measurements for analog core is done simultaneously with internal testing of digital cores. After this step, the analog core test results are reported in Announcement_Mode and the wrappers would be ready to set ExTest_Mode.

```
1. Initialization wrappers:
2.     Set DATC in Selt_Test_Mode;
3.     Set others in Bypass_Mode;
4. Internal_Test DATW;
5. Initialization wrappers:
6.     Set DATC in Initialization_Mode;
7.     Set others in Bypass_Mode;
8. Initialization DATW;
9.  Initialization wrappers:
10.    Set DATC in Start_Measure_Mode;
11.    Set others in Bypass_Mode;
12. Start Measurement;
13. For i:=1 to (M−1) do
14.  Initialization wrappers:
15.    Set WIR(i) InTest_Mode;
16.    Set others in Bypass_Mode;
17.  InTest Core i;
18. End for;
19. Initialization wrappers:
20.    Set DATC in Announcement_Mode;
21.    Set others in Bypass_Mode;
22. Report DATW results;
23. Initialization wrappers:
24.    Set in all wrappers in ExTest_Mode;
25. ExTest;
```

Fig.13 Sequential test scheduling algorithm

The concurrency in testing of analog and digital cores presented in this algorithm reduces the test application time for A/MS SoC.

EXPERIMENTAL RESULTS

To demonstrate the results of the proposed method, we present the application of the SR DfT wrapper for deep analog terminals in a cost effective manner. For the experimental setup, we have used three digital SoCs from the ITC'02 SoC test benchmarks, namely d695, h953 and g1023. We have added the dual-tone multifrequency receiver consisting of eight different biquadratic filters to the SoCs and refer to the mixed-signal SoCs as d695ms, h953ms and g1023ms.

Table 3 shows the SR DfT test time results for the eight biquadratic filters.

The test cost for a specified SoC-level TAM width can be expressed as follows:

$$Cost=\alpha_T C_T+\alpha_A C_A, \quad (11)$$

where α_T is the cost weighting factor for the test application time C_T, and α_A is the cost weighting factor for the area overhead cost C_A. The weighting factors are defined such that $\alpha_T+\alpha_A=1$.

Table 3 The SR DfT results for eight filters

Filter No.	Measured amplitude	Measured frequency	Testing time (clock cycles)
1	50	197	1070
2	128	201	1083
3	19	161	924
4	28	146	864
5	33	126	782
6	25	102	693
7	92	17	650
8	36	60	520

According to the proposed method, we consider two issues to minimize the test cost:

(1) To reduce the test hardware overhead cost, we propose a reconfigurable wrapper, the hardware of which can be shared by adjacent analog cores. In our example, we share one SR DfT between eight filters by duplicating a set of constant registers. The implementation of the SR DfT wrapper has been synthesized with 0.5 μm ASIC technology. The post-synthesis hardware overhead for the SR DfT wrapper without sharing and with sharing is 8832 gates and 1224 gates, respectively. The reconfigured wrapper shows 12.9% reduction in area overhead.

(2) The constant registers of the reconfigured SR DfT are initialized in Initialization_Mode and used sequentially in the Measure_Mode. The test results are saved in a set of flip-flops and are reported to chip pins in the Announcement_Mode. Because of the concurrency in testing of analog and digital cores, as discussed in the test scheduling algorithm, and sharing the wrapper, the test application time cost is decreased. Table 4 shows the comparison of test time (in clock cycles) and test cost for the mixed-signal SoCs using serial scheduling versus the proposed method. The last column shows the test cost reduction percentages for given $\alpha_I=\alpha_A=0.5$.

Table 4 The comparison of test time (in clock cycles) and test cost for mixed-signal SoCs using serial scheduling versus the proposed method

A/MS SoC	Serial scheduling without sharing	Our deep analog test method	Reduction in test time (%)	Reduction in test cost (%)
d695ms	59 971	48 715	18.8	15.85
h953ms	266 758	245 359	8.0	10.45
g1023ms	80 722	62 201	22.9	17.90

CONCLUSION

We have presented a cost effective approach for accessing to deep analog terminals within a mixed-signal SoC. Our wrapper design is a scalable and reconfigurable oscillation-based analyzer and is completely compatible with digital core-based test methodologies. Based on our proposed test scheduling algorithm, the concurrency of the test application for analog and digital cores reduces the test application time. At the same time, because of the reconfigurability of the design, the test hardware overhead cost is reduced by sharing SR DfT between several adjacent analog cores. Applying the proposed method to several SoCs that include eight deep analog filters showed the cost effectiveness of this approach.

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