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New design of sense amplifier for EEPROM memory*

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Abstract: We present a new sense amplifier circuit for EEPROM memory. The topology of the sense amplifier uses a voltage sensing method, having low cost and low power consumption as well as high reliability. The sense amplifier was implemented in an EEPROM realized with an SMIC 0.35-μm 2P3M CMOS embedded EEPROM process. Under the condition that the power supply is 3.3 V, simulation results showed that the charge time is 35 ns in the proposed sense amplifier, and that the maximum average current consumption during the read period is 40 μA. The novel topology allows the circuit to function with power supplies as low as 1.4 V. The sense amplifier has been implemented in 2-kb EEPROM memory for RFID tag IC applications, and has a silicon area of only 240 μm^2.

Key words: EEPROM, Sense amplifier (SA), Voltage sensing, Bidirectional conduction
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INTRODUCTION

EEPROM memories are used as storage devices for a wide variety of equipment, such as smart cards, mobile telephones, and microcontrollers. The portable microelectronics systems and smart cards require EEPROM memory with high speeds in both read and write operation modes as well as low power consumption (Haraszti, 2001; Conte *et al*., 2005). For example, the need for very low power dissipation and low cost has become a key design aspect for RFID tag IC (Barnett and Liu, 2007; Pillai *et al.*, 2007).

The power dissipation of the EEPROM is composed of static power, reading power, and writing power (Liu *et al.*, 2006). Read power dissipation is mainly caused by the sense amplifier (SA). There have been many publications on the design of EEPROM (Otsuka and Horowitz, 1997; Haraszti, 2001; Daga *et al*., 2003; Canet *et al.*, 2004; Xu *et al.*, 2004; Palumbo and Pappalardo, 2006; Walsh and Scott, 2006; Regnier *et al.*, 2006; Barnett and Liu, 2007; Na *et al.*, 2007; Raguet *et al*., 2007; Sergey and Sergey, 2007). However, there are almost no technical papers regarding the design of voltage SAs using a voltage sensing method. Conventional SAs are based on the current sensing method. This paper describes the design of a novel topology SA for EEPROM memories, capable of reducing the read power dissipation and satisfying high speed and low cost constraints. We show that by using a voltage sensing method, better circuit performance is achieved.

In Section 2 some drawbacks of conventional SAs are analyzed. In Section 3, a new SA circuit using a voltage sensing method is proposed. Simulation results are presented in Section 4 and conclusions in Section 5.

CONVENTIONAL SENSE AMPLIFIERS

There are many publications that treat the design of conventional SAs based on the current sensing method shown in Fig.1 (Otsuka and Horowitz, 1997; Haraszti, 2001; Daga *et al.*, 2003; Xu *et al.*, 2004). In this circuit, ‘0’ and ‘1’ are distinguished by using a differential circuit to compare a read out current with a reference current. The circuit has some drawbacks:

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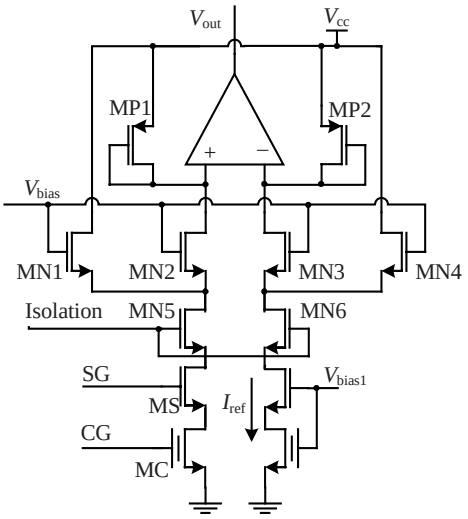

Fig.1 Conventional sense amplifier

(1) The conventional SA circuit needs a large reference current I_{ref}. To distinguish between '0' and '1', the reference current is typically the average of the read out currents for '0' and '1' data. For reliability, a reference current of tens of μA is needed (Otsuka and Horowitz, 1997; Xu *et al.*, 2004). For instance, Otsuka and Horowitz (1997) used a reference current of 32.9 μA. So, if a parallel read operation is performed, the conventional SA circuit will result in a large read out current $I_r \in (nI_{ref}, 3nI_{ref})$, where n is the number of bits read out in parallel.

(2) Characteristic degeneration of the floating gate transistor will change the '0' and '1' current levels and thus make the ideal choice of I_{ref} something other than the initial average of the read out currents for '0' and '1' (Canet *et al.*, 2004). This results in a smaller difference between the read out current and the reference current for one level or the other and increases the time required for sensing.

(3) The conventional SA circuit has many floating nodes that store charge. Hence it is essential to use an extra control logic circuit that correctly manages charge stored on key nodes that could otherwise cause incorrect read out.

VOLTAGE SENSE AMPLIFIERS

This paper proposes a new SA circuit using voltage sensing as shown in Fig.2. The SA is composed of charge controlling and voltage sensing circuits. The memory cell consists of a floating gate transistor MC and a select transistor MS.

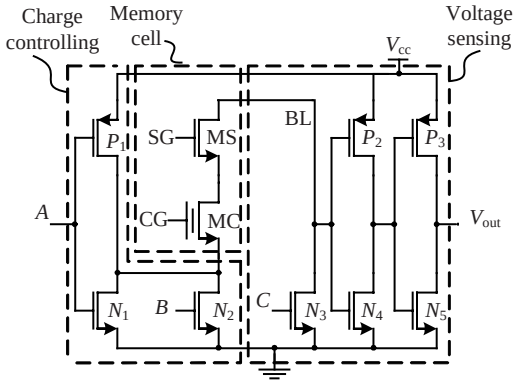

Fig.2 Proposed sense amplifier

Definition 1 The threshold voltage of the MC is p when storing a '0' signal, and q when storing a '1' signal. Fig.2 shows that the operation states of this SA are controlled by the three control terminals: *A*, *B* and *C*.

(1) Out-of-work state: *A*, *B* and *C* are all '1' to ensure that the drain and source of the memory cell are at low level.

(2) Work state: The control gate (CG) is $V_{CG}=(p+q)/2$ and the select gate (SG) is V_{cc}. Initially, *C* and *B* are set to '0' to turn off N_2 and N_3. Then, *A* is set to '0'. Here, when the stored signal of MC is '0', $V_{out}=0$; when the stored signal is '1', the BL (bit line) is charged to

$$V_{BL} = \min(V_{cc}-V_{tms}, V_{CG}-V_{tmc}), \quad (1)$$

where V_{tms} is the threshold of MS, and V_{tmc} is the threshold of MC. A '1' will be generated correctly at V_{out} as long as

$$V_{BL}>V_{cc}/2. \quad (2)$$

In Fig.2, the bidirectional conduction between the drain and source of MOS transistors is used for sensing the stored voltage ('0'/'1') at MC (Miyawaki *et al.*, 1994). High accuracy over sense voltage is achieved by using well-suited circuits with no floating nodes. The circuit topology of the SA, without bias circuit, enables costs to be minimized. The parasitic capacitance at the drain of N_3 is used as the

charging load. The threshold voltage of the inverter, composed of NMOS transistors N_4, N_5 and PMOS transistors P_2, P_3, can be amended to decrease the voltage charged. This results in a shorter time for charging the selected BL and makes the read power dissipation lower. Furthermore, by using a voltage sensing rather than a current sensing method, the proposed voltage SA is capable of resisting the characteristic degeneration of the floating gate transistor.

In one read process, the transient current and charges for charging are described, respectively, by the following equations:

$$\frac{\partial(V_{\mathrm{BLT}}C_{\mathrm{N3}})}{\partial t}=\beta(V_{\mathrm{CG}}-V_{\mathrm{tmc}}-V_{\mathrm{BLT}})^2, \tag{3}$$

$$\int_0^T \beta(V_{\mathrm{CG}}-V_{\mathrm{tmc}}-V_{\mathrm{BLT}})^2\,\mathrm{d}t=C_{\mathrm{N3}}(V_{\mathrm{CG}}-V_{\mathrm{tmc}}), \tag{4}$$

where V_{BLT} is the transient voltage of the BL, C_{N3} is the parasitic capacitance at the drain of N_3, and T is the charging time, $\beta=\mu_{\mathrm{n}}C_{\mathrm{ox}}W/(2L)$. Using Eqs.(3) and (4), the average charging time and current can be obtained during one read period.

IMPLEMENTATION AND SIMULATION RESULTS

The SA presented in previous sections was integrated in a 2-kb EEPROM memory fabricated in an SMIC 0.35-μm 2P3M CMOS embedded EEPROM process. In this design, the memory array is divided into 4 pages of 64 (8×8) bytes each. This arrangement, which needs 8 SAs, increases the speed of storing data because the erase and write operations of the page can be worked as a whole. One byte consists of eight memory cells (Fig.3). The read or write process of the whole EEPROM memory operates on a byte-by-byte basis. The SGs for all cells in a memory word are connected, as well as the CG. The SG signal linked to the WORDLINE controls the connection between the CG and the peripheral circuits, which avoids mistakes in the write procedure. In the 8 SAs, the sources of all floating gate transistors can be connected for sharing a charge controlling circuit (Fig.2). This reduces the chip size.

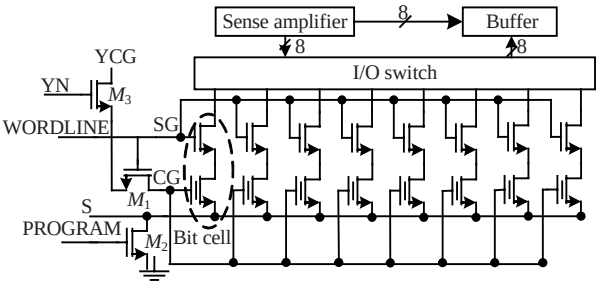

Fig.3 EEPROM memory array of one byte

The 25 °C operating conditions for the EEPROM memory cell implemented in the SMIC 0.35-μm process can be summarized as follows. The threshold voltage of the floating gate transistor MC is 4 V when storing a '0' signal, and −1 V when storing a '1' signal. From Eq.(1), we can see

$$V_{\mathrm{BL}}=\min(V_{\mathrm{cc}}-V_{\mathrm{tms}},\ 1.5-V_{\mathrm{tmc}}). \tag{5}$$

Under the condition that V_{cc} is 3.3 V, the SA was simulated for the worst case condition where all the 8 memory cells of one byte are in the '1' state. The resulting current waveforms are shown in Fig.4. I_{cc} and I_{cn} are the current consumptions of the conventional SA and the proposed SA, respectively. The charge time was 35 ns in the proposed SA, and the maximum average current consumption during the read period was 40 μA for the maximum clock speed of 28.57 MHz. Normally, the EEPROM chip works at a clock speed of 3.39 MHz, which is a quarter of sub-frequency of 13.56 MHz. Compared to the conventional SA current of about 400 μA, this is a significant improvement. With a 3.3-V power supply, the output data (V_{out}) for the new SA are shown in

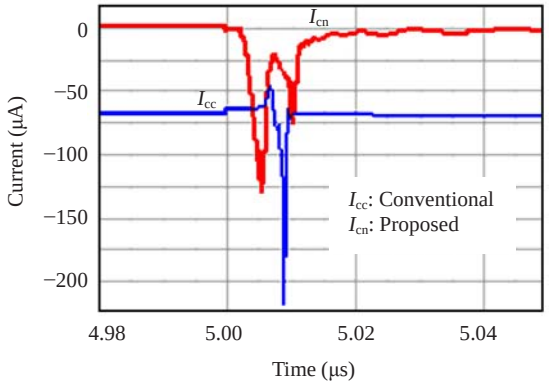

Fig.4 Simulation waveforms of the current consumptions for SA when a memory cell is '1'

Fig.5. Generally, the required working temperature range of the RFID tag is from −25 °C to 85 °C. The effect of temperature on power was very small. The simulation result showed that the power differentiation of the highest and lowest temperatures compared with 27 °C was 0.23% and 0.38%, respectively.

Furthermore, depending on the principle of the memory cell, $V_{CG}=(p+q)/2$ in Eq.(5) is the best value for voltage sensing and a lower voltage can be set for V_{CG}. By Eq.(2) and regulating the threshold voltage of the inverter in Fig.2, the proposed SA is capable of operating at voltages as low as 1.4 V. The V_{out} data for a 1.4-V power supply are shown in Fig.6. Here, the average current consumption during the read period

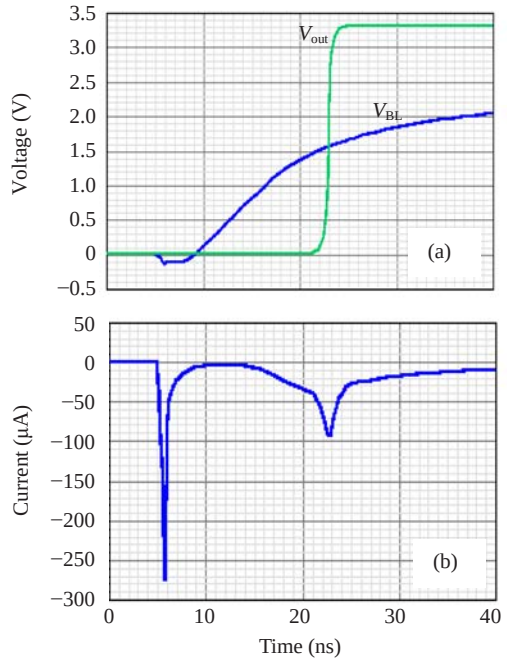

Fig.5 Simulation results of SA under a 3.3-V power supply. (a) Simulation results of V_{out} and V_{BL}; (b) Simulation waveform of the current consumption

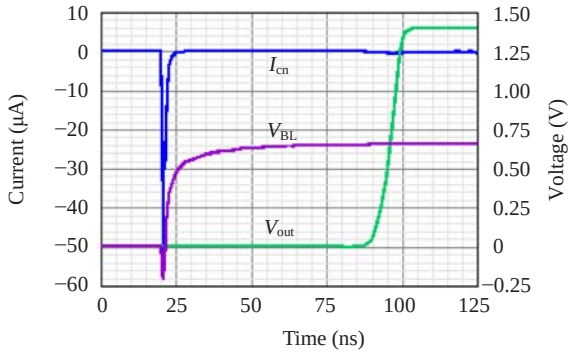

Fig.6 Simulation results of the sense amplifier under a 1.4-V power supply

was only 745 nA for the maximum clock speed of 14.08 MHz. This feature can be used for some electronic systems focused on low voltage and low power, not high speed. In this paper, the proposed SA is implemented only with a power supply of from 2.5 to 5 V (typically 3.3 V). The SA has a silicon area of about 240 μm^2 and its microphotograph is shown in Fig.7.

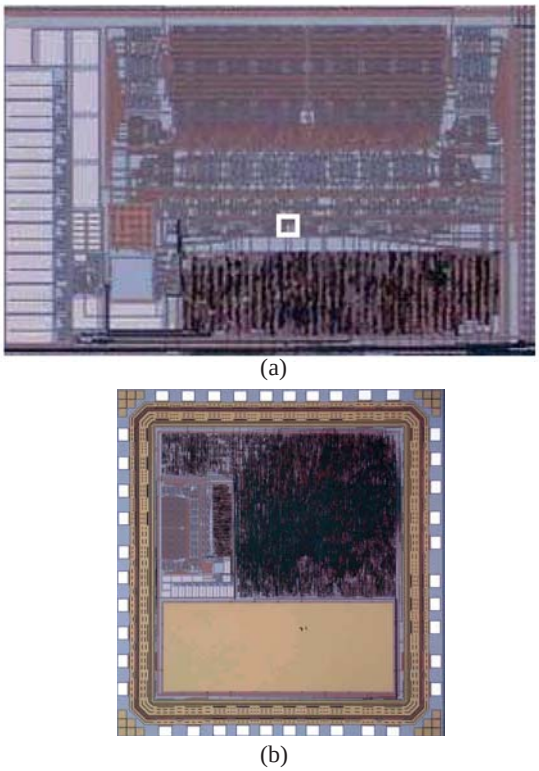

Fig.7 (a) The sense amplifier microphotograph (inside the bold pane) in 2-kb EEPROM memory; (b) The tag IC microphotograph

CONCLUSION

A new SA circuit using a voltage sensing method was designed and fabricated using the SMIC 0.35-μm 2P3M CMOS embedded EEPROM process. The bidirectional conduction between the drain and source of MOS transistors is used for sensing the stored voltage (‘0’/‘1’) at the floating gate transistor. The circuit is capable of operating over a wide voltage range (typically 2.5~5 V), and can function with power supplies as low as 1.4 V.

The SA was implemented in 2-kb EEPROM memory for RFID tag IC applications and improved significantly the read power dissipation with 40-μA read current.

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