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Design of a low power GPS receiver in 0.18 μm CMOS technology with a ΣΔ fractional-N synthesizer*

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Abstract: A 19 mW highly integrated GPS receiver with a ΣΔ fractional-N synthesizer is presented in this paper. Fractional-N frequency synthesizer architecture was adopted in this work, to provide more degrees of freedom in the synthesizer design. A high linearity low noise amplifier (LNA) is integrated into the chip. The radio receiver chip was fabricated in a 0.18 μm complementary metal oxide semiconductor (CMOS) process and packaged in a 48-pin 2 mm×2 mm land grid array chip scale package. The chip consumes 19 mW (LNA1 excluded) and the LNA1 6.3 mW. Measured performances are: noise figure<2 dB, channel gain=108 dB (LNA1 included), image rejection>36 dB, and −108 dBc/Hz @ 1 MHz phase noise offset from the carrier. The carrier noise ratio (C/N) can reach 41 dB at an input power of −130 dBm. The chip operates over a temperature range of [−40, 120] °C and ±5% tolerance over the CMOS technology process.

Key words: GPS receiver, ΣΔ fractional-N synthesizer, Image rejection, Phase noise
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1 Introduction

The global positioning system (GPS) was developed in the 1970s and 1980s by the U.S. Department of Defense primarily for use by the U.S. military. However, civil applications of GPS grew at an astonishing rate. GPS is now well on its way to becoming an essential part of the commercial and public infrastructure (IEEE Global History Network, 2008). A single-chip GPS designed in CMOS technology has been proposed for several years and has now been achieved (Peczalski, 2002; Gramegna *et al.*, 2006; Chung *et al*., 2008; Wang *et al*., 2008). The mass market is ready for the introduction of the GPS.

This paper presents the detailed design of a GPS radio front-end receiver with a CMOS ΣΔ fractional-N frequency synthesizer and provides the measurement results of the chip.

2 GPS radio architecture

Depending on the frequency plan, there are two basic approaches for collecting digitized GPS signal data. The first, called direct digitation, is to digitize the input signal at the L1 (1575.424 MHz) frequency directly (Di, 2008). The second, called the down-converted approach, is to down-convert the input signal to an intermediate frequency and then digitize it. Direct digitization has one main disadvantage: the amplifiers used must operate at a high frequency and thus can be expensive (Tsui and Akos, 1996). In this case, the analog-to-digital converter (ADC) needs to have a large input bandwidth to accommodate the

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high input frequency and this is difficult to build. Also, it is difficult to build a narrow-band filter at a higher frequency, and this kind of filter has relatively high insertion loss (Kim *et al*., 1999; Magoon *et al*., 2002). In the down-converted approach, the input frequency is converted to a much lower frequency called the intermediate frequency (IF). Hence, building a narrow-band filter with low insertion loss is much easier. The amplifiers which operate at a lower frequency are less expensive. The low IF center frequency should be selected carefully. When the center frequency is too high, the cost will be high as described above, but when the center frequency is too low, the $1/f$ noise of the devices substantially corrupts the signal, a severe problem in metal oxide semiconductor (MOS) implementations. However, if the stages following the mixer in the channel operate at relatively low frequencies, the magnitude of flicker noise can be minimized by adopting very large devices. Low-IF architecture, therefore, is the best approach for a CMOS implementation. The −130 dBm GPS L1 signal energy is located in a 2 MHz bandwidth centered at 1575.42 MHz. The architecture of the low IF frequency approach used in this device is shown in Fig. 1.

The first component following the antenna can be either a filter or an amplifier. However, the insertion loss of a filter is relatively high, about 2–3 dB, and it is bulky (Liu and Amin, 2008). Usually, a GPS receiver without special interfering signals in the neighborhood uses an amplifier as the first component after the antenna to obtain a low noise figure.

The output from the LNA2 is mixed down to the intermediate frequency filter (IFF) by an image rejection mixer. An IF of $4f_0$ (f_0=1.023 MHz) is the best trade-off between the gain×bandwidth in the IFF and flicker noise in the mixer. The sampling rate of the ADC is $16f_0$.

An external crystal oscillator (TCXO) is needed to provide the frequency from 13 to 26 MHz to the synthesizer. The synthesizer consists of an analog part and a digital part. The analog part includes the charge pump, the loop filter, and the voltage controlled oscillator (VCO). The digital part contains the division control logic—the ΣΔ modulator, the multi-modulus pre-scaler, and the phase frequency detector (PFD). The VCO oscillates at twice the required frequency and quadrature signals are derived by means of a divider by 2. A ΣΔ modulator is used to associate the realization of the fractional-N synthesizer. By moving the quantization error to the high frequency, the modulator can greatly reduce the power of in-band noise. Meanwhile, dither technology is used to flatten the spur generated by the ΣΔ modulator.

3 Circuit implementation

3.1 LNA1

The first component following the antenna is the LNA1, which has been integrated into the radio chip in this device. The LNA1 consumes less power when the single-ended mode is chosen. The other required

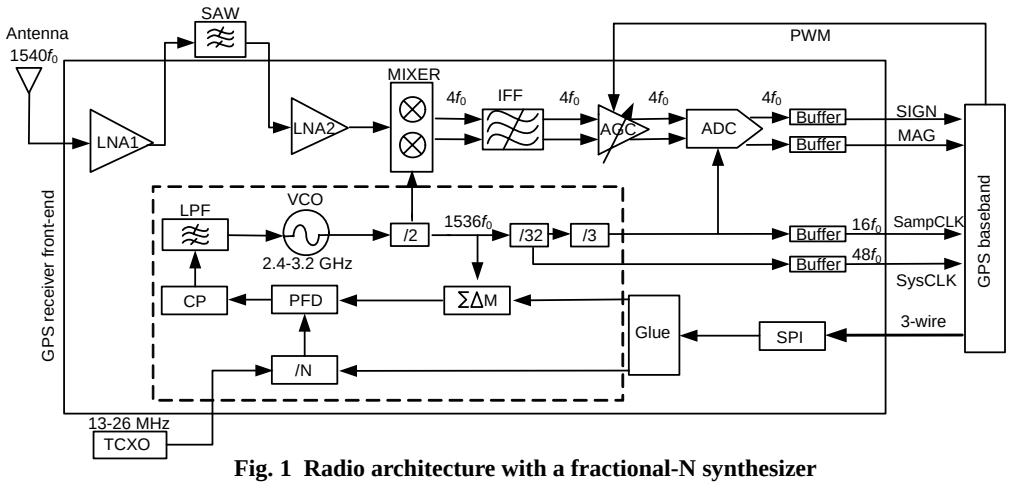

Fig. 1 Radio architecture with a fractional-N synthesizer

The synthesizer section is enclosed within the dotted rectangle and the intermediate frequency architecture is enclosed within the larger rectangle. SAW: surface acoustic wave; PWM: pulse width modulation; LNA: linearity low noise amplifier; IFF: intermediate frequency filter; LPF: low pass filter; VCO: voltage controlled oscillator; PFD: phase frequency detector; ADC: analog-to-digital converter; TCXO: external crystal oscillator; SPI: serial peripheral interface; AGC: automatic gain control; SIGN: sign of the signal; MAG: magnitude

specifications of the LNA1 in this design are low noise figure, large power gain, and high linearity. The LNA1 has a noise figure of 1.3 dB, a gain of 17.9 dB, and an input 1 dB compression point of −13 dB. The LNA1 consumes 5.6 mA from a power supply of 1.8 V.

3.2 LNA2 and MIXER

The design of the LNA2 and the image rejection mixer in this paper is shown in Fig. 2. There is a trade-off in the design of the LNA2 among low noise figure, large gain, high linearity, and low power dissipation. Noise generated by the transistor M_1 dominates the overall noise power of the LNA2. However, transistor M_3 contributes noise as well. Hence, the size of M_1 will affect the performance of the LNA2 directly. M_3 is used to isolate the input and output, and maintain the stability of the circuit. An inductor and capacitor (LC) tank maximizes the gain at the required frequency.

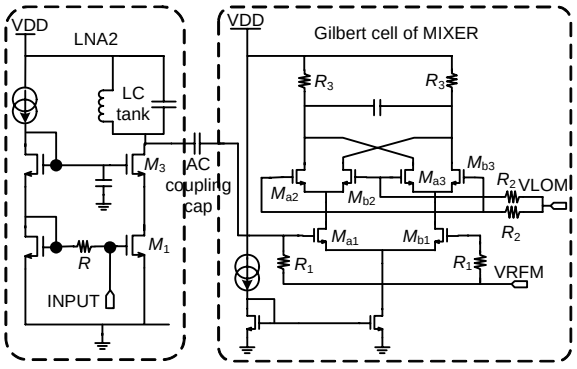

Fig. 2 LNA2 and the Gilbert cell used in the image rejection mixer

The mixer is AC coupled to the LNA2 and implements the Gilbert cell. It converts the radio frequency signal from 1.575 GHz ($1540f_0$) down to an IF of 4.092 MHz ($4f_0$). The image rejection mixer, which consists of two Gilbert cells, has the advantage of high conversion gain, low noise figure, and good isolation between IF signal and RF and local oscillator (LO) signals. The mixer (Fig. 2) provides only one Gilbert cell circuit but there is an identical one, which is not shown in Fig. 2. Image rejection of the mixer is 37 dB across the 2 MHz band, and of the LNA2-MIXER P1dB is 3.8 dBm. The linearity and power dissipation were optimized by careful design. In this design, the LNA2-MIXER features noise figure=4 dB, gain=30 dB and draws 4 mA from a 1.8 V supply.

3.3 ΣΔ fractional-N synthesizer

In ΣΔ fractional-N frequency synthesizers, the input of the ΣΔ modulator is a constant so-called DC value which is a bit-stream with a fractional mean value equal to the input value of the modulator (Rhee *et al*., 2000; Ti *et al*., 2008). In this design, a multi-stage noise shaping (MASH) 1-1-1 ΣΔ modulator (Fig. 3) has been adopted consisting of three first-order modulators, whose quantization error E_i is the input to the next modulator. By summing the filtered versions of the first-order outputs co_i, the quantization errors of the first and second modulators are cancelled (Zhu *et al*., 2004; Xiao *et al*., 2008). Since the ΣΔ modulator in the fractional-N phase-locked loop (PLL) is an all digital implementation, the cancellation is perfect. The output spectrum of the ΣΔ modulator is shown in Fig. 4. As the ΣΔ modulator used in the synthesizer would cause fractional spurs, dither technology was used to flatten the spurs and then the ΣΔ mechanism modulates the flattened noise. The modulated noise at high frequency is then filtered by the loop filter of the PLL.

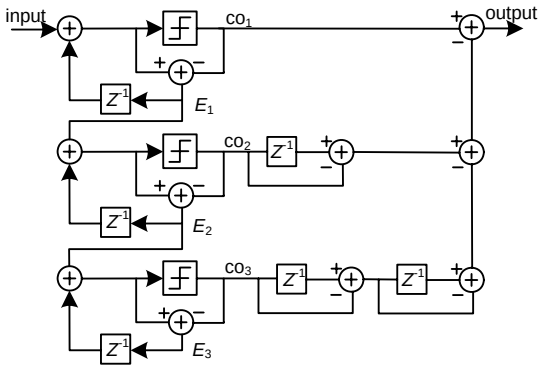

Fig. 3 The multi-stage noise shaping (MASH) 1-1-1 ΣΔ modulator

In this design, the VCO provides a frequency range from 2.958 to 3.318 GHz. To cover such a frequency range, an LC multi-band switch VCO is needed. Consequently, an automatic digital VCO calibration is needed for selecting the desired target frequency. An on-chip inductor using pattern ground shield (PGS) was adopted to ensure high Q and good noise isolation. The architecture also needs high LO amplitude buffers to be correlated with the mixer to ensure high performance. Complementary NMOS and PMOS LC tank VCO has been adopted in this design. A circuit schematic of the VCO in this design

is shown in Fig. 5. In this architecture, the DC current can be re-used and it is easy to design because no center-tap is needed for the inductor. The phase noise is 6 dB better than that of a cross-coupled NMOS or PMOS LC tank VCO. For a low power GPS application, this architecture is the best choice. Furthermore, the design can be optimized according to the Leeson equation (Huang *et al*., 2007; Bruzdzinski *et al*., 2008). The features of the VCO and LO in this design are shown in Table 1.

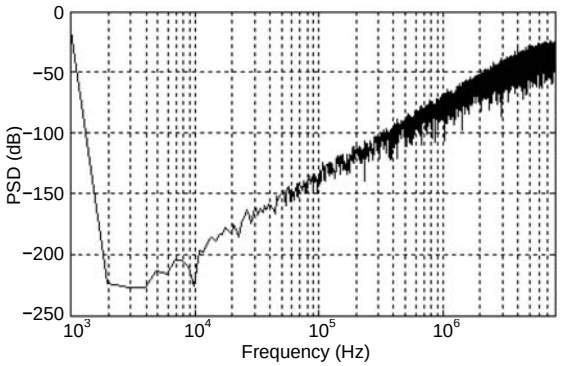

Fig. 4 Output noise power spectral density (PSD) of the multi-stage noise shaping (MASH) modulator

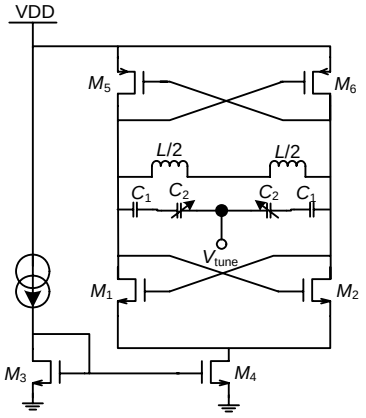

Fig. 5 Complementary NMOS and PMOS LC tank VCO

Table 1 Features of the VCO and LO

Parameter	Specification	Comments
VCO cover frequency	2.958–3.318 GHz	±5% over process
VCO output amplitude	300 $mV_{p\text{-}p}$	Differential output
LO phase noise	−80 dBc/Hz	@ 100 Hz and in-band
	−108 dBc/Hz	@ 1 MHz
	−120 dBc/Hz	@ 3 MHz
	−128 dBc/Hz	@ 10 MHz
VCO start time	<10 μs	
K_{VCO}	45 MHz/V	High band
	25 MHz/V	Low band
VCO tuning voltage	0.4–1.6 V	
VCO supply sensitivity	30 MHz/V	@ 1.8 V

VCO: voltage controlled oscillator; LO: local oscillator; K_{VCO}: sensitivity of VCO

3.4 IFF, AGC, and 2-bit ADC

The IF filter implements a 6th-order Chebyshev transfer function with $4f_0$ center frequency and provides an anti-aliasing function before the baseband ADC. It is based on the cascade of three similar low-pass cells (Fig. 6). Since there is an AC coupling capacitor between the mixer and the IF filter, the IF filter provides a pass-band behavior. The −3 dB bandwidth of the IF filter in this design is from 4 to 7 MHz with an active gain of 13 to 16 dB. The roll-off factor is larger than 20 dB at 28 MHz and the gain flatness is controlled in the range of −1 to +1 dB.

The automatic gain control (AGC) has a wide dynamic range from −2 to 52 dB with a gain step of 1.7 dB in this device. After receiving the feedback pulse-width signal from the baseband, the gain of the AGC changes accordingly. The default gain of AGC is 30 dB (Aloi, 2007).

A 1-bit quantization of the baseband signal is provided by most current GPS receivers. However, the binary phase shift keying (BPSK) direct frequency

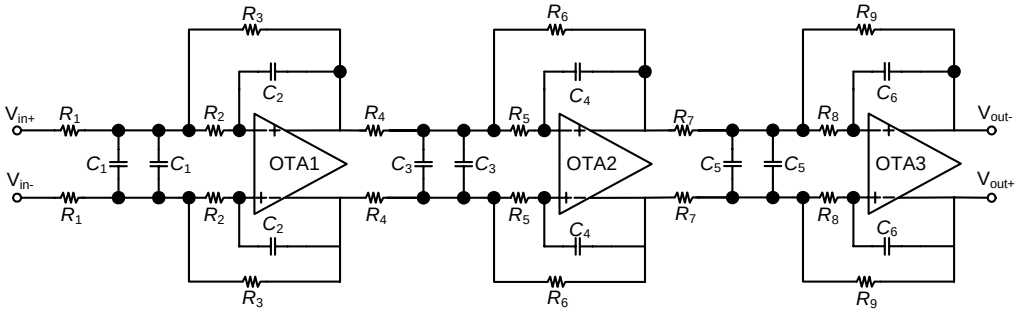

Fig. 6 Intermediate frequency (IF) filter architecture

spread spectrum signal is affected by Gaussian noise of the GPS receiver, and an SNR degradation of about 1.96 dB can be introduced by a 1-bit ADC. In this work, a 2-bit ADC was adopted and its output consists of SIGN (sign of the signal) and MAG (for magnitude) (Fig. 7). The threshold for MAG is 50 mV and the offset error for SIGN has a range from −4.8 to 4.0 mV in this design.

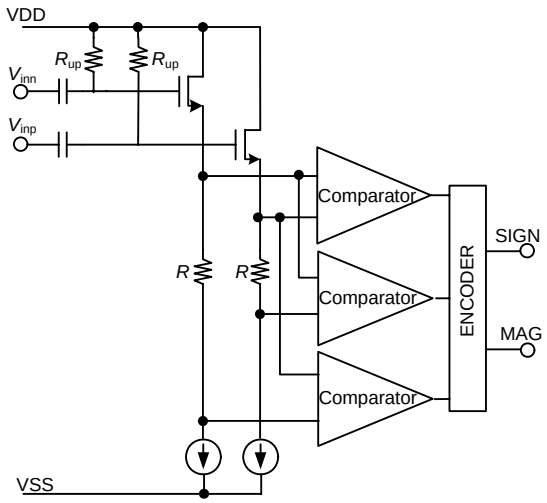

Fig. 7 The two-bit analog-to-digital converter (ADC) architecture

4 Experimental results

The circuit was fabricated in a 0.18 μm CMOS process. The temperature range is [−40, 120] °C and in the typical condition it draws 10.5 mA from a supply voltage in the [1.7, 1.9] V range. A summary of radio channel measured parameters is shown in Table 2.

Table 2 Main specifications of the receiver

Parameter	Measurement result
Channel gain (including LNA1)	108 dB
Noise figure of LNA1	1.3 dB
S11 (LNA1 input port)	−15 dB
S11(LNA2 input port)	−12 dB
Input P1dB of LNA1	−13 dBm
Image rejection (center-of-band)	36 dB
PLL phase noise @ 100 kHz	−80 dBc/Hz
PLL phase noise @ 1 MHz	−108 dBc/Hz
IF filter bandwidth	6.5 MHz
AGC gain dynamic range	54 dB
AGC gain step	1.65–1.85 dB
ADC threshold voltage	50 mV
Current dissipation (without LNA1)	10.5 mA

The measured output spectrum of the fractional-N synthesizer and phase noise performance are shown in Figs. 8 and 9, respectively. The local oscillator is locked at the center frequency of 1.571 42 GHz and the phase noise at 1 MHz is −108 dBc/Hz with the baseband turned off. The signal spectrum of the AGC output is shown in Fig. 10. The strength of input signal of the LNA2 is −110 dBm and there is a −47 dB attenuator following the AGC.

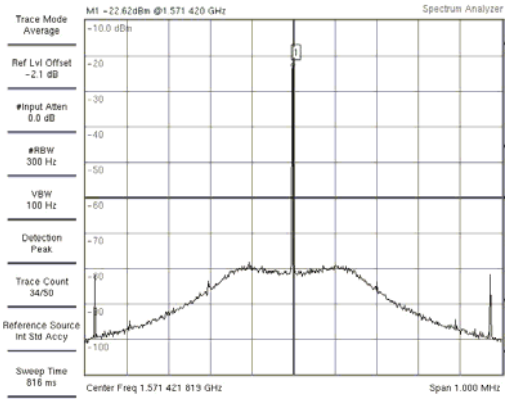

Fig. 8 Measured output spectrum of the fractional-N synthesizer

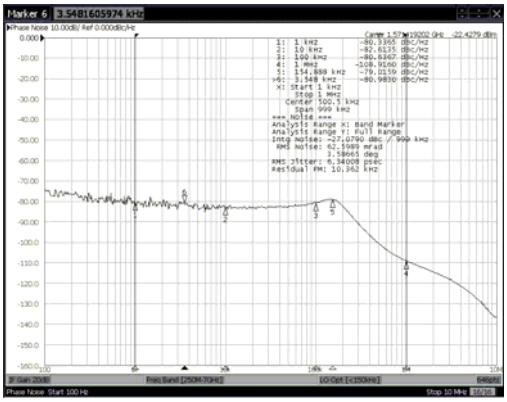

Fig. 9 The PLL phase noise with baseband turned off

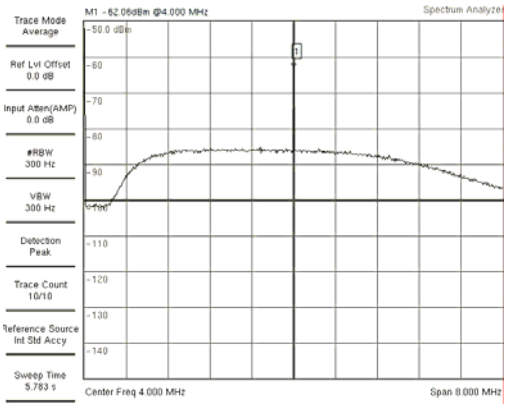

Fig. 10 Signal spectrum of the AGC output

5 Conclusions

A low power, highly integrated and versatile GPS receiver is presented in this paper. The power dissipation of the LNA1, LNA2, MIXER, AGC, ADC, and frequency synthesizer has been optimized. The devices in the circuits have been designed to be as small as possible to meet the low cost requirement. The chip shown in Fig. 11 can operate in a temperature range of [−40, 120] °C, ±5% tolerance over the CMOS technology process and draws 10.5 mA without the LNA1.

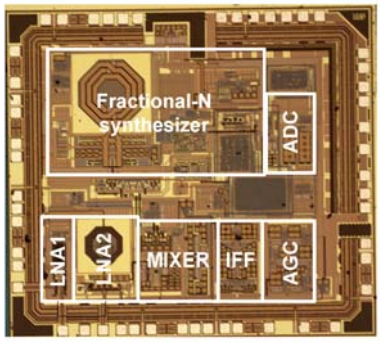

Fig. 11 GPS receiver chip microphotograph

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