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Generalized multilevel current source inverter topology with self-balancing current

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Abstract: A generalized single-phase multilevel current source inverter (MCSI) topology with self-balancing current is proposed, which uses the duality transformation from the generalized multilevel voltage source inverter (MVSI) topology. The existing single-phase 8- and 6-switch 5-level current source inverters (CSIs) can be derived from this generalized MCSI topology. In the proposed topology, each intermediate DC-link current level can be balanced automatically without adding any external circuits; thus, a true multilevel structure is provided. Moreover, owing to the dual relationship, many research results relating to the operation, modulation, and control strategies of MVSIs can be applied directly to the MCSIs. Some simulation results are presented to verify the proposed MCSI topology.

Key words: Multilevel current source inverter (MCSI), Topology, Self current balancing, Duality
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1 Introduction

Compared to two-level inverters, multilevel inverters have enormous benefits for higher power applications (Rodriguez *et al.*, 2009), including reduced harmonics and increased power ratings because of reduced switching device voltage and current stresses. Until now, multilevel voltage source inverters (VSIs) (Rodriguez *et al.*, 2002; McGrath and Holmes, 2009) have been the focus of attention, despite the fact that current source inverters (CSIs) have some advantages over VSIs for higher power applications. These include more stable operating conditions, direct control of the output current, faster dynamic response in some circumstances, and easier fault management. The storage elements in CSIs are inductors, which have the disadvantages of higher conduction losses and lower energy storage efficiency compared to DC-link capacitors, and thus the applications for CSIs are limited. However, some of the disadvantages of traditional inductors can now be overcome owing to the development of superconducting magnetic energy storage (SMES) technology (Steurer *et al.*, 2003), and hence their use is becoming more attractive, especially for very large current applications.

A generic *N*-level CSI topology was proposed and an 8-switch 5-level CSI system was analyzed in detail by Antunes *et al.* (1999). Xiong *et al.* (2004) presented an alternative 8-switch 5-level topology for single-phase application, which was extended to three-phase operation by Xiong *et al.* (2005). Bao *et al.* (2006b) proposed a reduced 6-switch 5-level CSI topology with the obvious advantages of only 6 switches and only one intermediate DC-link inductor, which was also extended to three-phase applications by Bao *et al.* (2006a). Regardless of the specific multilevel CSI (MCSI) topology that is used, the common issue for these multilevel inverters is how to control effectively the magnitude of the 1/2-level

intermediate DC-link current. Without current balancing control, the current cannot be maintained at a constant level. A similar problem is found with the intermediate DC-link voltage in a three-level neutral point clamped (NPC) VSI (Cobreces *et al.*, 2009) if some type of compensation control is not considered. In this respect, the three existing MCSIs are not real multilevel structures because they all need auxiliary circuits for current balancing control.

By using the duality transformation from the generalized MVSI topology, a generalized MCSI topology with the ability to self-balance current can be constructed. The existing single-phase 8-switch and 6-switch 5-level CSIs can all be derived from the generalized MCSI topology by simplification. Moreover, at any number of current levels, the intermediate DC-link current level can be automatically balanced without adding any auxiliary circuits, and thus a real multilevel structure is achieved. Research results relating to the operation, modulation, and control strategies of MVSIs (McGrath and Holmes, 2002; Chan *et al.*, 2009; Gao *et al.*, 2009**)** can be applied directly to the MCSI owing to the dual relationship.

In this paper, the conformation method, circuit structures, and self-balancing current principle of the generalized MCSI topology are presented. Simulation results are given to verify the proposed MCSI structure.

2 Conformation of a single-phase multilevel current source inverter

The duality transformation can be applied directly to those circuits which are in planar forms (Freeland, 1992; Agelidis and Joos, 1993), so it is possible to construct the single-phase MCSIs from the single-phase MVSIs.

Fig. 1 shows the generalized single-phase 5-level VSI topology, which is composed of the generalized 3-level inverter phase legs (Peng, 2001). Owing to its planar property, the duality transformation can be used directly. The corresponding dual structure, namely the generalized single-phase 5-level CSI topology, is obtained (Fig. 2) in which the switch in parallel with a diode is transformed into a switch in series with a diode through duality. The clamped-capacitor's dual component is a sharing-inductor which acts as the current source.

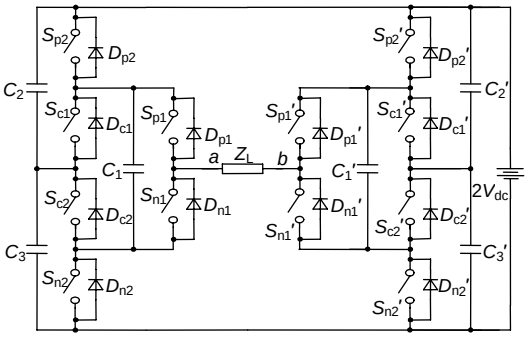

Fig. 1 The generalized sine-phase 5-level VSI topology

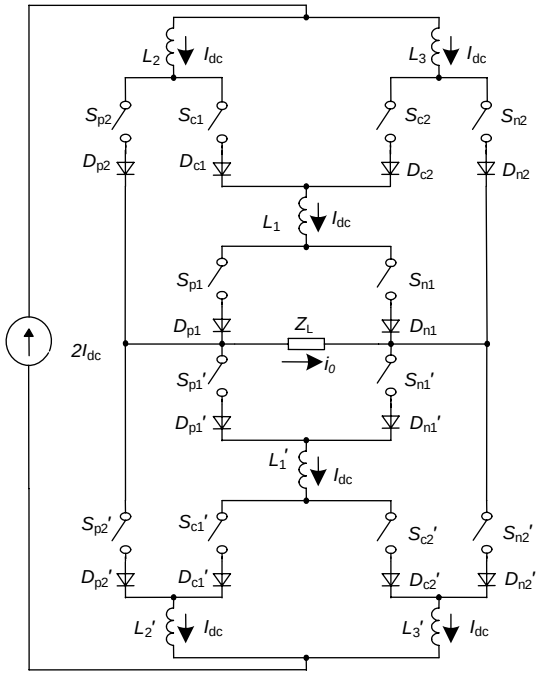

Fig. 2 The generalized single-phase 5-level CSI topology

Similarly, by using dual transformation, a single-phase CSI topology with any odd number of levels, can be derived from the generalized MVSI topology with the corresponding voltage levels. However, if the level number is greater than five, the network graph becomes more complex and it is time consuming to construct MCSI topology using dual conversion in the usual way. For simplicity, a complex *N*-level inverter can be divided into several basic 2-level voltage cells. The generalized *N*-level phase leg (Peng, 2001) can be looked upon as a horizontal pyramid of the basic 2-level voltage cells (Fig. 3). Similarly, according to the circuit duality, a generalized *N*-level CSI can be constructed by the basic 2-level current cell, which is the dual component of

the basic 2-level voltage cell. There is no need to conform MCSI topology by applying the dual transformation to the whole MVSI topology.

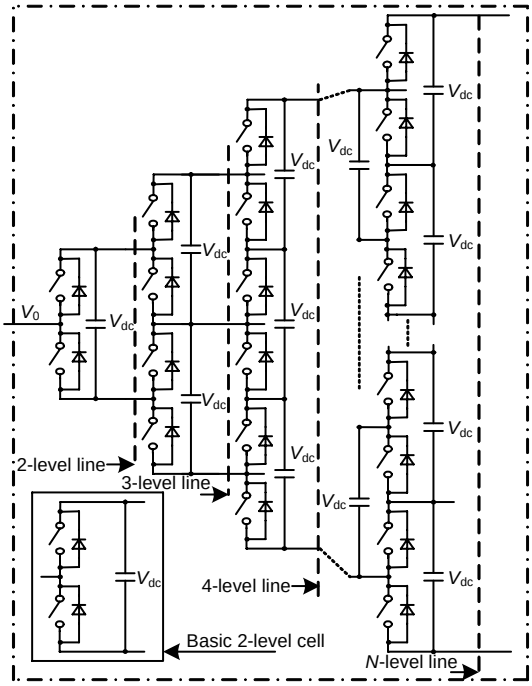

Fig. 3 Phase leg of the generalized *N*-level VSI
Inset: basic 2-level voltage cell

The basic 2-level voltage cell is shown in the inset of Fig. 3, as a dual, and the basic 2-level current cell is shown in the inset of Fig. 4. In each switch pole (between two level lines) of Fig. 3, the basic 2-level voltage cells are in series connection, as a dual. The basic 2-level current cells are in parallel with each other to form higher level current cells (between two level lines) in Fig. 4. In Fig. 3, the two adjacent switch poles are connected in parallel through clamping-capacitors, and any two adjacent high-level current cells are connected in series as a dual through sharing-inductors (Fig. 4). The generalized *N*-level phase leg, which can be regarded as a vertical pyramid of the basic 2-level current cells, is shown in Fig. 4.

By proper combination of the generalized phase leg, a single-phase CSI with any odd number of levels, including the conventional three-level inverter, can be obtained. By connecting the two *N*-level phase legs along the horizontal axis (load line) symmetrically, a generalized (2*N*−1)-level single-phase CSI can be derived. For instance, a three-level inverter phase leg is obtained by cutting off at the '3-level line'. Taking these two three-level phase legs in symmetric conjunction along the horizontal axis (load line), a generalized single-phase 5-level CSI can be obtained, with the topology shown in Fig. 2.

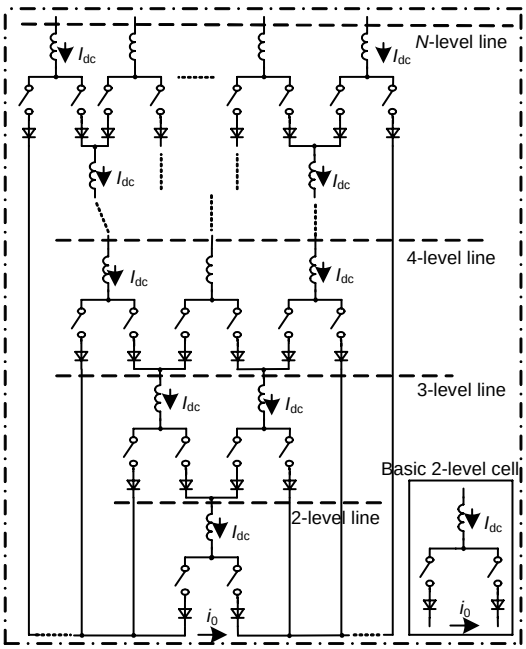

Fig. 4 Phase leg of the generalized *N*-level CSI
Inset: basic 2-level current cell

Fig. 5 shows two dual structures of specific MVSIs that can be deduced from the generalized MCSI. By eliminating all the clamping active switches in Fig. 2, the dual structure of a 5-level diode-clamped VSI is derived (Fig. 5a). Fig. 5b shows the dual structure of a 5-level flying-capacitor VSI made by eliminating all the clamping switches and diodes. Because the sharing-inductors L_2 and L_3, and L_2' and L_3' are in parallel directly, they do not contribute to current balancing and can be removed. Thus, a single-phase 8-switch 5-level CSI (Antunes *et al*., 1999) can be derived. For further simplification, a reduced 6-switch 5-level CSI topology (Bao *et al*., 2006b) can be obtained by eliminating a basic 2-level cell on the basis of 8-switch 5-level CSI topology.

3 Operation analysis

Since the MCSI topology obtained is completely dual to the generalized MVSI, the relationship between the output voltage and the switching states of

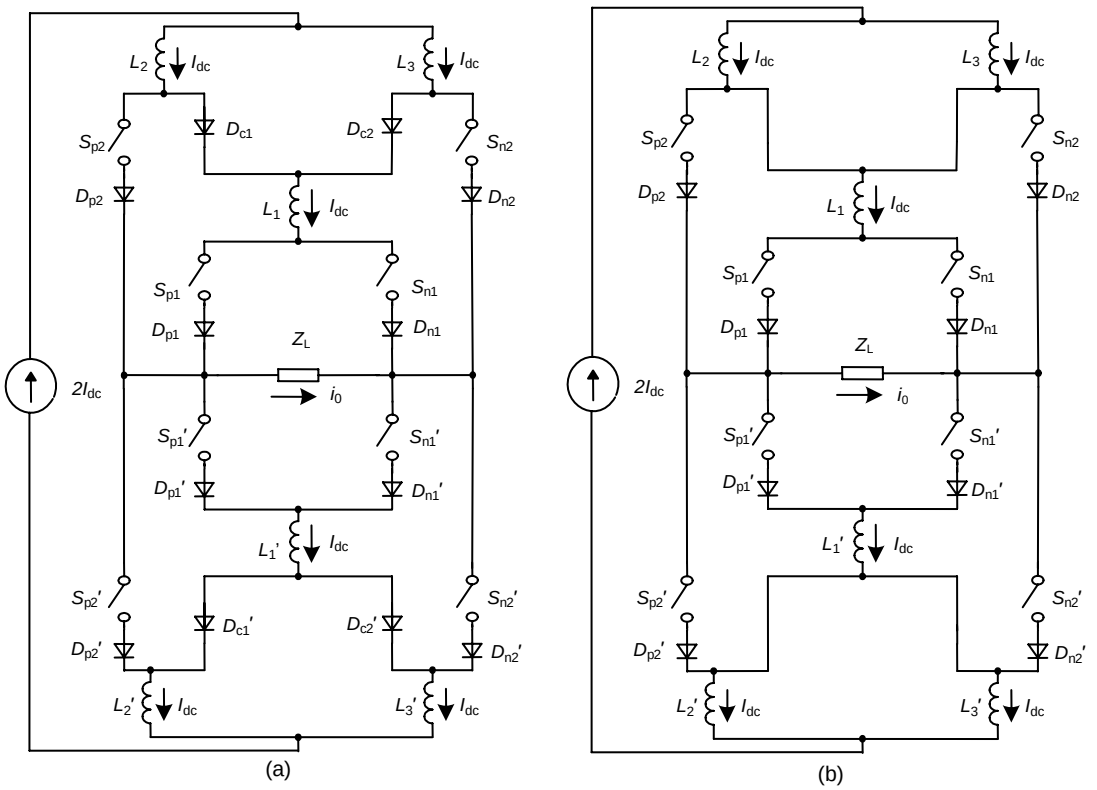

Fig. 5 The derived single-phase 5-level CSI topologies
(a) Dual structure of a diode-clamped VSI; (b) Dual structure of a flying-capacitor VSI

the MVSI can be mapped directly to the generalized MCSI. Without loss of generality, taking the generalized 5-level CSI (Fig. 2) as an example, the total DC current source $2I_{dc}$ is equally divided by sharing-inductors: L_2, L_3, L_2', and L_3'. Any two paralleled two switches that are connected to the same node of each sharing-inductor are complementary, and there are a total of 8 switch-pairs: (S_{p2}, S_{c1}), (S_{n2}, S_{c2}), (S_{c1}, S_{c2}), (S_{p1}, S_{n1}), (S_{p2}', S_{c1}'), (S_{n2}', S_{c2}'), (S_{c1}', S_{c2}'), and (S_{p1}', S_{n1}'). The current flowing through each component, including the active switch, diode, and sharing-inductor, is $I_{dc}/2$. Table 1 lists the states of S_{p1}, S_{p2}, S_{p1}', and S_{p2}' that generate $+2I_{dc}$, $+I_{dc}$, 0, $-I_{dc}$, and $-2I_{dc}$ current levels. If the states of S_{p1}, S_{p2}, S_{p1}', and S_{p2}' are determined, then the states of all the remaining switches are unique according to the complementary rule.

From the above, to achieve the proper multilevel current waveforms at the AC output, the currents flowing through all sharing-inductors must be kept well balanced. In the generalized MVSI, all voltage levels can be self-balanced through clamping switches and clamping diodes. As a dual, in the generalized MCSI, all current levels should be self-balanced through current-sharing switches by using switching state redundancies. Therefore, the mechanism of inductor current self-balance is similar to that of capacitor voltage self-balance (McGrath and Holmes, 2008).

Table 1 Switch states of the generalized 5-level CSI

i_0	S_{p1}	S_{p2}	S_{p1}'	S_{p2}'
$+2I_{dc}$	1	1	0	0
$+I_{dc}$	1	1	0	1
	1	1	1	0
	0	1	0	0
	1	0	0	0
0	1	1	1	1
	0	0	0	0
	1	0	1	0
	1	0	0	1
	0	1	1	0
	0	1	0	1
$-I_{dc}$	0	0	0	1
	0	0	1	0
	0	1	1	1
	1	0	1	1
$-2I_{dc}$	0	0	1	1

Table 2 lists all possible inductor branches when generating different current levels. The specific inductor branch is determined by the switching states of S_{c1}, S_{c2}, S_{c1}', and S_{c2}'. For example, when switch S_{c1} is gated on, the inductors L_1, L_2 are connected in series to make their currents uniform; when switch S_{c2} is gated on, the inductors L_1, L_3 are connected in series to keep their currents uniform. Similarly, when the switches S_{c1}' and S_{c2}' are gated on, the currents flowing through the inductors L_1' and L_2', and L_1' and L_3' can be well balanced. From Table 2, the switching state used for generating $i_0=+2I_{dc}$ or $i_0=-2I_{dc}$ is unique, while there are other switching states for producing $i_0=+I_{dc}$, $i_0=-I_{dc}$, and $i_0=0$. For instance, there are four alternative switching states and three different inductor branches that produce $i_0=+I_{dc}$ (Table 2). Therefore, it is possible to balance the inductors' currents by selecting the inductor branches consecutively at each switching moment.

Table 2 Switch states versus inductor branches

i_0	Conducting switches	Inductor branches*	Sequence
$+2I_{dc}$	S_{p1} S_{p2} S_{c2} S_{n1}' S_{n2}' S_{c1}'	$(L_1+L_3)//L_2$, $(L_1'+L_2')//L_3'$	3
$+I_{dc}$	S_{p1} S_{p2} S_{c2} S_{p2}' S_{n1}' S_{c2}'	$(L_1+L_3)//L_2$, $(L_1'+L_3')//L_2'$	4
	S_{p1} S_{p2} S_{c2} S_{p1}' S_{n2}' S_{c1}'	$(L_1+L_3)//L_2$, $(L_1'+L_2')//L_3'$	
	S_{p2} S_{n1} S_{c2} S_{n1}' S_{n2}' S_{c1}'	$(L_1+L_3)//L_2$, $(L_1'+L_2')//L_3'$	
	S_{p1} S_{n2} S_{c1} S_{n1}' S_{n2}' S_{c1}'	$(L_1+L_2)//L_3$, $(L_1'+L_2')//L_3'$	2
0	S_{p1} S_{p2} S_{c2} S_{p1}' S_{p2}' S_{c2}'	$(L_1+L_3)//L_2$, $(L_1'+L_3')//L_2'$	1
	S_{n1} S_{n2} S_{c1} S_{n1}' S_{n2}' S_{c1}'	$(L_1+L_2)//L_3$, $(L_1'+L_2')//L_3'$	5
	S_{p1} S_{n2} S_{c1} S_{p1}' S_{n2}' S_{c1}'	$(L_1+L_2)//L_3$, $(L_1'+L_2')//L_3'$	
	S_{p1} S_{n2} S_{c1} S_{p2}' S_{n1}' S_{c2}'	$(L_1+L_2)//L_3$, $(L_1'+L_3')//L_2'$	
	S_{p2} S_{n1} S_{c2} S_{p1}' S_{n2}' S_{c1}'	$(L_1+L_3)//L_2$, $(L_1'+L_2')//L_3'$	
	S_{p2} S_{n1} S_{c2} S_{p2}' S_{n1}' S_{c2}'	$(L_1+L_3)//L_2$, $(L_1'+L_3')//L_2'$	
$-I_{dc}$	S_{n1} S_{n2} S_{c1} S_{p2}' S_{n1}' S_{c2}'	$(L_1+L_2)//L_3$, $(L_1'+L_3')//L_2'$	
	S_{n1} S_{n2} S_{c1} S_{p1}' S_{n2}' S_{c1}'	$(L_1+L_2)//L_3$, $(L_1'+L_2')//L_3'$	8
	S_{p2} S_{n1} S_{c2} S_{p1}' S_{p2}' S_{c2}'	$(L_1+L_3)//L_2$, $(L_1'+L_3')//L_2'$	6
	S_{p1} S_{n2} S_{c1} S_{p1}' S_{p2}' S_{c2}'	$(L_1+L_2)//L_3$, $(L_1'+L_3')//L_2'$	
$-2I_{dc}$	S_{n1} S_{n2} S_{c1} S_{p1}' S_{p2}' S_{c2}'	$(L_1+L_2)//L_3$, $(L_1'+L_3')//L_2'$	7

* '+' means the inductors are in series with each other; '//' means the inductor branches are in parallel connection

Fig. 6 shows one possible switching sequence in a whole fundamental period for producing 5-level output currents. According to the level numbers, one fundamental period is divided into eight sections. In each operation section, two sharing-inductors will be connected in series to balance their currents by gating on S_{cx} or S_{cx}' (x=1, 2). The output current $i_0=+I_{dc}$ can be produced in both sections (2) and (4). In section (2), $i_{L1}=i_{L2}$, and $i_{L1}'=i_{L2}'$, while in section (4), $i_{L1}=i_{L3}$, and $i_{L1}'=i_{L3}'$. Therefore, $i_{L1}=i_{L2}=i_{L3}$ and $i_{L1}'=i_{L2}'=i_{L3}'$ are implemented respectively by choosing the alternative inductor branches. In this way, all the sharing-inductors' currents can be balanced.

Of course, to avoid being operated in fault situations, the current flowing through all the sharing-inductors should be maintained at any moment. Therefore, besides the switching sequence listed above, an extra switching sequence for protecting the whole MCSI system should be added, that is, gating on all switches. In such fault situations, the self-balancing of 1/2-level current will be lost.

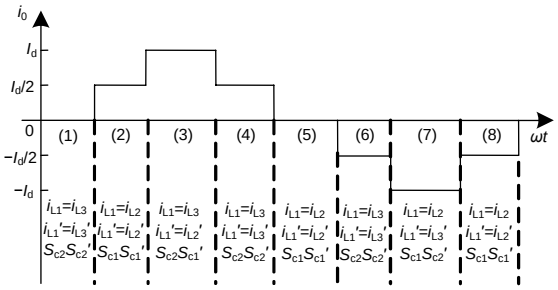

Fig. 6 One possible switching sequence for current self-balance

4 Simulation results

To verify the operation of this generalized single-phase multi-level CSI, a simulation system of a generalized single-phase 5-level CSI was set up based on MATLAB/SIMULINK. The main parameters used in this single-phase 5-level CSI were as follows: the DC current source $2I_{dc}$ was 100 A; the switches were made up using MOSFETs in series with fast recovery diodes; the sharing-inductors $L_x=L_x'=50$ mH (x=1, 2, 3). The switching strategy shown in Fig. 6 was applied for self-balancing the current.

Fig. 7 shows some simulation waveforms of the generalized single-phase 5-level CSI operated with different load types. In Figs. 8a–8c, i_{L1}, i_{L2}, and i_{L3} are the currents flowing through the sharing-inductors L_1, L_2, and L_3, respectively. Clearly, they are very close to one half of $2I_{dc}$ except that a few current overshoots are seen during each switching state transition, which are caused by the alteration of inductor branches. Therefore, all the intermediate DC current levels can be well balanced even if operating with different

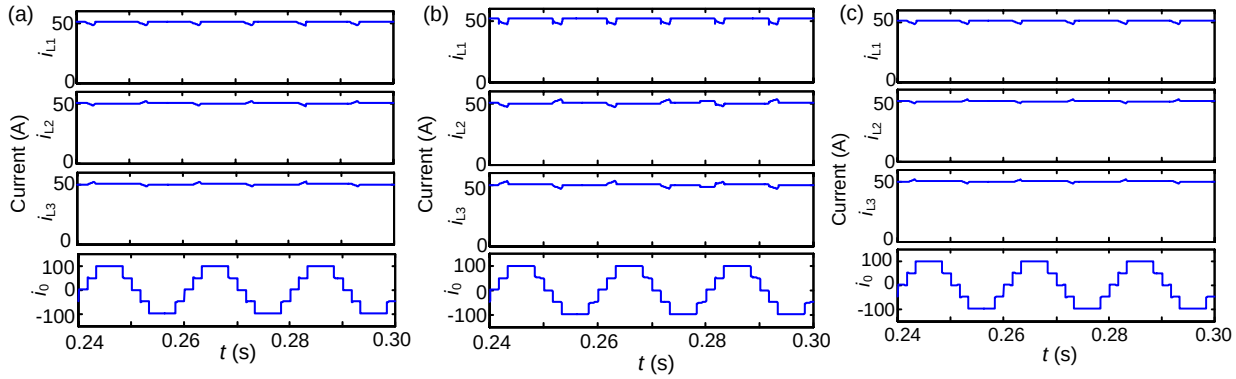

Fig. 7 Simulation waveforms of the generalized 5-level CSI

(a) R=5 Ω; (b) R=5 Ω, L=5 mH; (c) R=5 Ω, C=50 μF

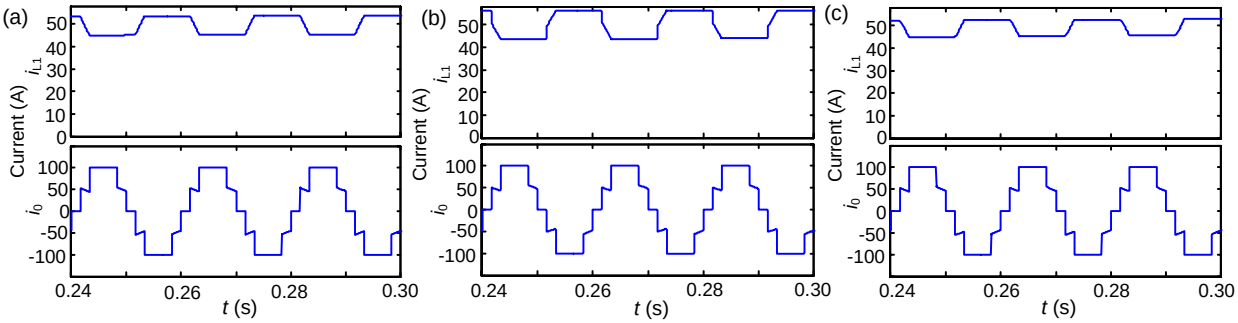

Fig. 8 Simulation waveforms of the 8-switch 5-level CSI

(a) R=5 Ω; (b) R=5 Ω, L=5 mH; (c) R=5 Ω, C=50 μF

load types. The 5-level output current waveform with symmetrical 1/2-level current was obtained, and is shown as i_0.

For comparison, the simulation system of an 8-switch single-phase 5-level CSI was also constructed based on MATLAB/SIMULINK. The main circuit parameters and the load parameters were the same as those used in the generalized single-phase 5-level CSI system. The asymmetric switching strategy described by Antunes *et al*. (1999) was used. In Figs. 8a–8c, i_{L1} is the current flowing through the sharing-inductor L_1. Although the average value of i_{L1} can be balanced at one half of $2I_{dc}$, a current ripple is clearly seen compared to that of i_{L1}, i_{L2}, and i_{L3} (Fig. 7). Therefore, the output current waveform will be distorted, which can be demonstrated by i_0. To achieve the proper multilevel current waveforms at the AC output, the current flowing through the sharing-inductor must be maintained at its appropriate DC value with the assistance of the current-balancing control (Bao *et al*., 2006b; Familiant *et al*., 2007).

5 Conclusions

We have presented a dual approach to the conformation of single-phase multilevel CSI topology. A new generalized single-phase 5-level CSI was derived by applying the direct duality to the generalized single-phase 5-level flying capacitors VSI. The existing single-phase 8-switch and 6-switch 5-level CSIs can be derived from this generalized MCSI topology by moderate simplification. The generalized multilevel inverter topology has the ability to balance each intermediate DC-link current, and shows the performance of a real multilevel structure, though the numbers of active switches and sharing-inductors are greater than those of the existing multilevel inverters. The results relating to operation, current balance, and pulse width modulation (PWM) strategies have been verified by simulation. Moreover, many research results relating to the operation, modulation, and control strategies of multilevel VSIs can be applied directly to the multilevel CSI owing to the dual relationship.

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