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An efficient PSP-based model for optimized cross-coupled MOSFETs in voltage controlled oscillator*

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Abstract: This paper proposes an efficient PSP-based model for cross-coupled metal-oxide-semiconductor field-effect transistors (MOSFETs) with optimized layout in the voltage controlled oscillator (VCO). The model employs a PSP charge model to characterize the bias-dependent extrinsic capacitance instead of numerical functions with strong non-linearity. The simulation convergence is greatly improved by this method. An original scheme is developed to extract the parameters of the PSP charge model based on *S*-parameters measurement. The interconnection parasitics of the cross-coupled MOSFETs are modeled based on vector fitting. The model is verified with an LC VCO design, and exhibits excellent convergence during simulation. The results show improvements as high as 60.5% and 61.8% in simulation efficiency and accuracy, respectively, indicating that the proposed model better characterizes optimized cross-coupled MOSFETs in advanced radio frequency (RF) circuit design.

Key words: Layout optimizing, Modeling, PSP, Charge model, Cross-coupled, Metal-oxide-semiconductor (MOS), Voltage controlled oscillator (VCO)
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1 Introduction

As wireless market extends to standards of wider bandwidths and higher frequencies, complementary metal-oxide-semiconductor (CMOS) voltage controlled oscillators (VCOs) with a higher frequency have gained increasing interest. Some works (Nakamura *et al.*, 2006; Heydari *et al.*, 2007; Chan *et al.*, 2008; Nagase *et al.*, 2010) have been carried out to optimize the layout of a metal-oxide-semiconductor field-effect transistor (MOSFET) to achieve higher cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}), which are sensitive to the parasitic capacitance (Doan *et al.*, 2005). However, only the layout effect of an individual n-type metal-oxide-semiconductor transistor (NMOS) is considered in these works, and in a cross-coupled NMOS pair, the interconnection parasitics between two devices may outweigh that of an individual NMOS. Moreover, considering the advantage of a symmetrical design which improves the VCO phase noise (Hajimiri and Lee, 1998), the layout of the minimum parasitic capacitance and high symmetry is essential in a high-performance VCO design; hence, the model for layout-optimized cross-coupled MOSFETs is needed. Practically, this model must take simulation efficiency and accuracy into account, and for large signal simulation, convergence is also a crucial figure of merit.

In an MOSFET, the extrinsic capacitance has a great impact on the radio frequency (RF) performance, which consists of extrinsic gate capacitance and junction capacitance. Generally, the extrinsic capacitance is bias-dependent and is not constant during a period of oscillation; thus, it has a great impact on the

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accuracy of frequency prediction in simulation. The model for junction capacitance is relatively simple and achieves convergence during simulation. The standard compact models derive the extrinsic gate capacitance behavior based on semi-empirical methods (Liu *et al.*, 1999) or physical methods (Li *et al.*, 2008); however, the lack of standard procedures for extracting model parameters has driven foundries to develop their own numerical fitting functions with strong non-linearities for this capacitance. These functions provide good numerical fittings in *S*-parameters. However, the excellent fitting in *S*-parameters does not guarantee accurate simulation of any non-linear circuit, as *S*-parameters are naturally small-signal parameters (Heydari *et al.*, 2007); on the other hand, the fitting functions of strong non-linearity have a poor physical basis and suffer from convergence problems, especially in periodic steady state (PSS) simulation.

This paper proposes an efficient model for layout-optimized cross-coupled MOSFETs in VCO, which considers cross-coupled MOSFETs as a unit device. A PSP charge model is used to characterize the bias-dependent extrinsic capacitance instead of numerical non-linear functions to improve the simulation convergence. An original scheme for the PSP charge model extraction is developed based on *S*-parameters measurements since there is no standard extraction procedure. The parasitic parameters introduced by interconnection are modeled with vector fitting (Gustavsen and Semlyen, 1999), which accelerates the circuit-level simulation compared with the normal post-layout parasitic extraction. This paper is arranged as follows: Section 2 gives a brief introduction to some extrinsic capacitance models. In Section 3, the optimized layout of the cross-coupled NMOS is investigated, followed by analysis of the equivalent circuits of both common-source NMOS and optimized cross-coupled pair. Subsequently, the PSP charge model extraction and interconnection parasitics are demonstrated. In Section 4, fitted curves of gate and gate-to-drain capacitance are presented after the PSP charge model is extracted. Interconnect admittance is extracted with vector fitting. Subsequently, an NMOS-only LC VCO is designed and fabricated to verify the simulation convergence, efficiency, and accuracy of the proposed model. Finally, conclusions are given in Section 5.

2 Brief overview of extrinsic capacitance modeling

In an MOSFET, the extrinsic capacitance consists of the extrinsic gate capacitance, C_{GDEX} and C_{GSEX}, as well as the drain/source-to-bulk junction capacitance, C_{JDB} and C_{JSB} (Fig. 1). The extrinsic gate capacitance is composed of fringe capacitance and overlap capacitance. Theoretically, the fringe capacitance consists of an outer portion as well as inner portion. BSIM3v3 considers the outer fringe capacitance as bias-independent while the inner as bias-dependent but usually comes under the overlap capacitance.

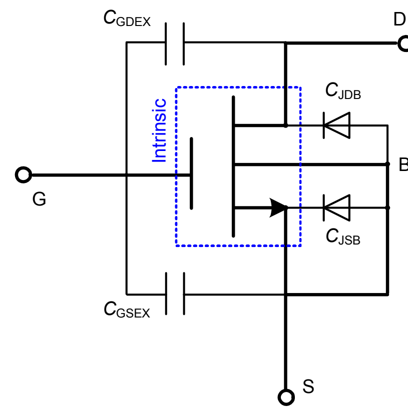

Fig. 1 Extrinsic capacitance of a common-source n-type metal-oxide-semiconductor transistor (NMOS)

As for the junction capacitance, it is generally considered as the diode capacitance. Since the drain-to-bulk (D-B) diode is inversely biased while the source-to-bulk (S-B) diode is shorted in most of circuit topology, the D-B junction capacitance is the dominated contributor of the junction capacitance, which is well modeled by (Liu *et al.*, 1999)

$$C_{\mathrm{JDB}} = C_{\mathrm{J}} \cdot \left(1 + M_{\mathrm{J}} \frac{V_{\mathrm{DB}}}{P_{\mathrm{B}}}\right), \tag{1}$$

where C_{J}, M_{J}, and P_{B} are bias-independent coefficients. This model seldom causes convergence problems during simulation since it has linear nature.

Unfortunately, the model of extrinsic capacitance at the gate is more complex and is treated differently in different standard models. BSIM3v3 divides the extrinsic gate capacitance into the

bias-independent fringe capacitance (strictly speaking, the outer fringe capacitance) and the bias-dependent overlap capacitance (overlap capacitance associated with the inner fringe capacitance). The bias-independent fringe capacitance is constant when the terminal voltage changes, and for bias-dependent overlap capacitance, accuracy and convergence of its model need to be carefully considered. For example, the BSIM models the overlap gate-to-drain capacitance, C_{GDOV} (per unit gate-width), as

$$C_{\mathrm{GDOV}}=\frac{\partial(Q_{\mathrm{D,overlap}}/W_{\mathrm{active}})}{\partial V_{\mathrm{GD}}}=\frac{\partial}{\partial V_{\mathrm{GD}}}\left\{\mathrm{CGD0}\cdot V_{\mathrm{GD}}+\mathrm{CGD1}\cdot\left[V_{\mathrm{GD}}-V_{\mathrm{GD,\,overlap}}-\frac{\mathrm{CKAPPA}}{2}\cdot\left(-1+\sqrt{1-\frac{4V_{\mathrm{GD,\,overlap}}}{\mathrm{CKAPPA}}}\right)\right]\right\},\quad(2)$$

$$V_{\mathrm{GD,\,overlap}}=\frac{1}{2}\left(V_{\mathrm{GD}}+\delta_1-\sqrt{(V_{\mathrm{GD}}+\delta_1)^2+4\delta_1}\right),\quad \delta_1=0.02V,\quad(3)$$

where CGD0, CGD1, and CKAPPA are model parameters. Eqs. (2) and (3) show weak non-linearities by introducing the square root, which will not change significantly as V_{GD} swings, nor will it cause a convergence problem.

PSP 102.3 has a different theory as it considers both the fringe and the overlap gate capacitance, C_{FR} and C_{GXOV}, respectively, as bias-dependent. According to the PSP extrinsic charge model (Li *et al.*, 2008), the extrinsic gate-to-drain capacitance, C_{FRD} and C_{GDOV}, are derived as

$$C_{\mathrm{GDOV}}=\frac{\partial Q_{\mathrm{D,\,overlap}}}{\partial V_{\mathrm{GD}}}=\frac{\partial\left(\mathrm{CGOVD}\cdot(V_{\mathrm{GS}}-V_{\mathrm{DS}}-\psi_{\mathrm{dov}})\right)}{\partial V_{\mathrm{GD}}},\quad(4)$$

$$C_{\mathrm{FRD}}=\frac{\partial Q_{\mathrm{FD,\,overlap}}}{\partial V_{\mathrm{GD}}}=\frac{\partial\left(\mathrm{CFRD}\cdot(V_{\mathrm{GS}}-V_{\mathrm{DS}})\right)}{\partial V_{\mathrm{GD}}},\quad(5)$$

where the surface potential at the overlap drain is given by

$$\psi_{\mathrm{dov}}=-\phi_{\mathrm{T}}x_{\mathrm{dov}}\left(-\frac{V_{\mathrm{GS}}-V_{\mathrm{DS}}}{\phi_{\mathrm{T}}}\right).\quad(6)$$

CGOVD and CFRD are model parameters, ϕ_{T} is the thermal voltage (kT/q), and x_{dov} (V) is a process-parameter-related function which is linear with regard to the terminal voltage. The PSP extrinsic charge model will not cause a convergence problem, either. Note that although C_{FRD} is bias-dependent, its bias sensitivity is much lower than that of C_{GDOV}, because the latter is also modulated by the surface potential at the overlap drain.

As mentioned before, foundries prefer to the models with extractable parameters. Sometimes, they choose numerical models rather than physical ones. To achieve accurate fittings in *S*-parameters, foundries often use functions with strong non-linearities, such as power and exponential functions and their combinations. One example is as follows:

$$C_{\mathrm{GDOV}}=\sum_{i=1}^{M}A_i(B_iV_{\mathrm{GS}}-C_iV_{\mathrm{DS}})^{D_i}+\sum_{j=1}^{N}AE_j\cdot\mathrm{e}^{BE_jV_{\mathrm{GS}}-CE_jV_{\mathrm{DS}}},\quad(7)$$

where the coefficients could be either positive or negative. The strong non-linearity is introduced by the power and exponential contributions. When this function is adopted in a large signal simulation, as the terminal voltage swings, the capacitance will change significantly under several specific voltages, and a convergence problem occurs. To be precise, the strong non-linearity of the numerical model ensures the accurate fitting in *S*-parameters, but it causes the convergence problem.

Although standard compact models provide reference models for the extrinsic gate capacitance based on semi-empirical or physical deduction, they seldom provide standard procedures to extract the model parameters. Additionally, an efficient extraction procedure is also one of the key aspects for the model implementation. In contrast, parameters in numerical fitting functions are easy to determine; however, these functions are suitable mainly for small-signal rather than large-signal simulations owing to their accuracy and convergence limitations.

3 Device layout, equivalent circuit, and the modeling method

The sample device is an NMOS of 22 fingers, 2 μm in width and 60 nm in length for each finger.

The optimized layout of the cross-coupled NMOS (de Ranter *et al.*, 2002) is shown in Fig. 2. Two NMOS are placed side by side, and the drain of one NMOS is connected directly to the gate of the other. This layout avoids the wide and long interconnection between the two NMOS in an ordinary cross-coupled configuration, which lowers the parasitic capacitance. Moreover, the two NMOS are much closer to each other, providing a better process uniformity, which improves the symmetry of the cross-coupled devices.

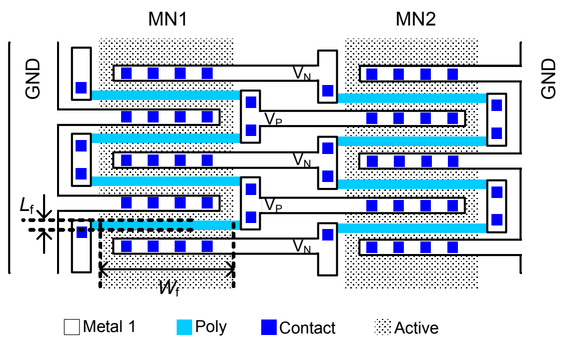

Fig. 2 Optimized layout of the cross-coupled NMOS (four fingers are presented for each NMOS)

Two-port equivalent circuits of the common source NMOS and its cross-coupled configuration are shown in Fig. 3. As shown in Fig. 3a, the gate-to-drain and the gate-to-source capacitances, C_{GD} and C_{GS}, respectively, consist of the intrinsic channel capacitance as well as the extrinsic capacitance, C_{GDEX} and C_{GSEX}. C_{GDEX} and C_{GSEX} are divided into components including overlap gate-to-drain, gate-to-source, and gate-to-bulk capacitors, C_{GDOV}, C_{GSOV}, and C_{GBOV}, respectively, as well as fringe capacitors at drain and source, C_{FRD} and C_{FRS}, respectively. A model is established with PSP 102.3 for this sample NMOS. In Fig. 3b, two NMOS are cross-coupled connected, and the admittances Y_P, Y_N, and Y_X refer to the interconnection parasitics at two ports of the NMOS and across them, respectively.

3.1 PSP charge model extraction

The PSP charge model is surface-potential-based, and characterizes the extrinsic capacitance as a supplement to capacitance-voltage (C-V) response of the intrinsic channel. Assuming the sample NMOS has symmetric drain and source, the extrinsic overlap and fringe capacitance on both sides are considered the same, which are characterized by parameter CGOV and CFR, respectively. For the symmetrical device, the parameters CGOVD in Eq. (4) and CFRD in Eq. (5) can be replaced with CGOV and CFR, respectively, which simplifies the extraction procedure. Subsequently, four charge model parameters are involved in modeling for the extrinsic capacitance, COX, CGOV, CGBOV, and CFR, which are listed in Table 1 (Li *et al.*, 2008).

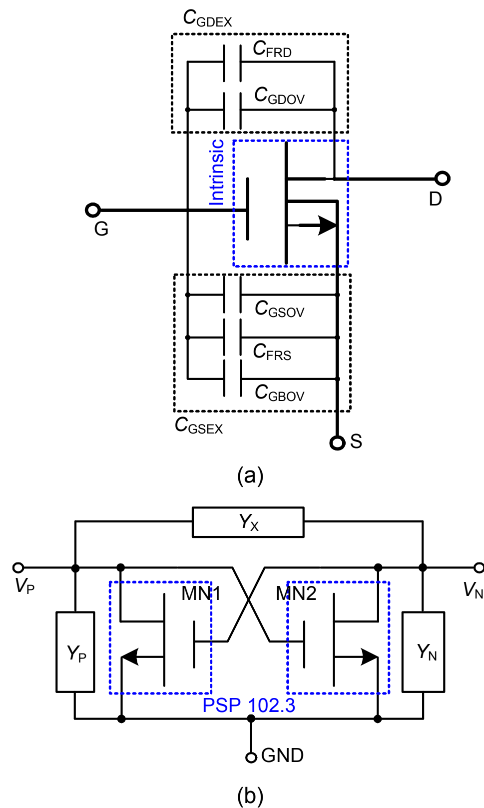

Fig. 3 Schematic of a common-source sample NMOS (a) and its cross-coupled configuration (b)

Table 1 PSP 102.3 charge model parameters used in this work

Parameter	Description
COX	Oxide capacitance for the intrinsic channel
CGOV	Oxide capacitance for the gate-drain/source overlap
CGBOV	Oxide capacitance for the gate-bulk overlap
CFR	Outer fringe capacitance

As shown in Fig. 3a, C_{GD} and C_{GS} can be extracted with imaginary parts of Y_{11} and Y_{12}, as follows (Kwon *et al.*, 2002):

$$C_{GD} = -\text{Im}[Y_{12}]/\omega, \tag{8}$$

$$C_{GS} = \left(\text{Im}[Y_{11}] + \text{Im}[Y_{12}]\right)/\omega, \tag{9}$$

$$C_{GG} = C_{GD} + C_{GS} = \text{Im}[Y_{11}]/\omega, \tag{10}$$

where ω refers to the frequency. Thus, $C_{GD}(V_G, V_D)$ is obtained from Y-parameters at a specified frequency using Eq. (8). The total gate capacitance C_{GG} is the sum of C_{GD} and C_{GS}; therefore, $C_{GG}(V_G)$ is obtained from Y-parameters at a specified frequency while V_D=0 from Eq. (10). The Y-parameters are derived from measured S-parameters. Hence, the charge model extraction flow is as follows:

1. Optimize COX and CFR to fit on curve $C_{GG}(V_G)$ at V_D=0.
2. Extract intrinsic parameters following the PSP standard procedure.
3. Optimize CGOV, CFR, and CGBOV to fit on curve $C_{GD}(V_G, V_D)$.
4. Optimize CGBOV to fit on curve $C_{GG}(V_G)$.

In Step 1, as the bias sensitivity of C_{FRD} is much lower than that of C_{GDOV}, C_{FRD} is considered as bias-independent when initializing the extraction.

Step 2 is important as it ensures that the intrinsic capacitance (also bias-dependent) is taken into account before extracting the extrinsic capacitance parameters from the total gate-to-drain capacitance. PSP derives intrinsic capacitance from COX and other process parameters related to doping and oxide thickness. According to the standard PSP extraction procedure, the parameter COX is extracted from the C_{GG} curve of an extra device with a long and wide channel by C-V measurement. Here, COX is extracted directly from the C_{GG} curve of the sample device by S-parameters measurement, which avoids process variations and errors introduced by two separated measurements of the extra device and the sample. This may improve the intrinsic capacitance extraction and C_{GG} fitting; however, without Steps 3 and 4, the extrinsic gate capacitance cannot be extracted and C_{GD} cannot be characterized.

3.2 Interconnection modeling

Interconnection parasitics are normally evaluated by the post-layout parasitics extraction, and modeled using a series of distributed resistor/inductor/capacitor (R/L/C) segments as shown in Fig. 4a. This large number of R/L/C segments will significantly slow down the post-layout simulation. Besides, the normal post-layout extraction can hardly evaluate interconnection accurately since the MOS layout is optimized, especially when the frequency is high. The vector fitting method, however, models the parasitics with a simple serial/parallel R/L/C network, which improves the simulation accuracy and efficiency. Although this method is numerical, it provides excellent fitting capability and adaptability for fast modeling of a passive device.

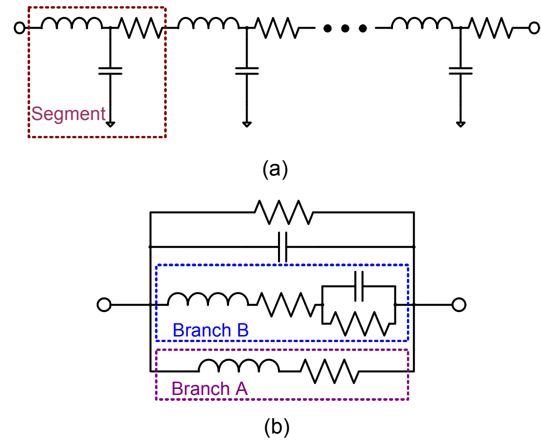

Fig. 4 Interconnection equivalent circuits synthesized by post-layout parasitic parameters extraction (a) and by vector fitting (b)
In (b), branches A and B are for adjusting poles. The more the branches added, the more the poles adopted, and the better the fitting obtained at higher frequency

Vector fitting is based on rational function approximation (Gustavsen and Semlyen, 1999). It introduces poles with different R/L/C branches and fits the transfer function $H(s)$ of the target admittance or impedance. In Fig. 4b, each branch A introduces one real pole, while each branch B introduces a pair of complex conjugate poles. Generally, branch A is sufficient for passive parasitics modeling, as this parasitics will have less fluctuation. The number of poles, or in other words, the number of branch A, is determined by the fitting accuracy. Branch B, however, is more capable of handling the fluctuation in device frequency response, and is more likely to be used in complex devices such as a transformer. The vector fitting is a numerical method, which sometimes causes the R/L/C value extracted to be negative; however, it will not cause a stability or a convergence problem.

Before extraction, the number of poles is determined according to the concerned frequency range. More poles mean that more of branches A and B are needed, which provides the capability fitting up to a higher operation frequency with certain accuracy. As observed from the structure symmetry shown in Fig. 3b, the terminal parasitic admittances, Y_P and Y_N, are considered identical. Subsequently, the interconnection parasitic admittances, Y_P, Y_N, and Y_X, are derived from interconnection Y-parameters as follows:

$$Y_P = Y_N = Y_{\text{interconnect.11}} + Y_{\text{interconnect.12}}, \quad (11)$$

$$Y_X = -Y_{\text{interconnect.12}}. \quad (12)$$

In Fig. 5, each part of the admittance is synthesized into a specific lumped R/L/C network in Fig. 4b, which is with four branches A and without branch B. Finally, the values of R, L, and C in the network can be determined by the vector fitting algorithm (Gustavsen and Semlyen, 1999).

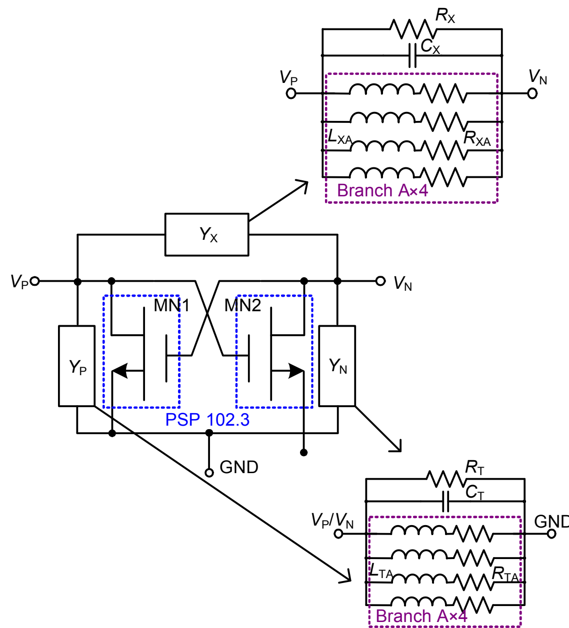

Fig. 5 Interconnect admittance synthesized into a specific lumped R/L/C network by vector fitting

4 Experimental results

The sample NMOS and layout-optimized cross-coupled pair are fabricated in a 65-nm CMOS process with a ground-signal-ground (GSG) test structure. Two-port S-parameters of the sample NMOS are measured on-wafer up to 40 GHz, then de-embedded by subtracting Y-parameters of the open GSG test structure and translated into $C_{GG}(V_G)$ and $C_{GD}(V_G, V_D)$ curves to extract the PSP charge model. Fig. 6 shows the fitting results of $C_{GG}(V_G)$ and $C_{GD}(V_G, V_D)$ curves at 1 GHz when charge model parameters are obtained, and then compares the situations with or without the extrinsic charge model. As shown in Fig. 6a, COX is well extracted directly from $C_{GG}(V_G)$ of the sample NMOS based on S-parameters measurement, and in Fig. 6b, the bias-dependent gate-to-drain capacitance is well characterized by the PSP charge model. Simulation results without the PSP extrinsic charge model is also shown in Fig. 6. As the parameters CGOV, CFR, and CGBOV are set to zero, $C_{GG}(V_G)$ and $C_{GD}(V_G, V_D)$ drop by about 5×10^{-15} F. This capacitance drop indicates that the extrinsic capacitance has a great impact on the device performance at the RF range, and the extraction of the intrinsic capacitance parameter COX will be influenced. Except for the capacitance drop, the $C_{GD}(V_G, V_D)$ pattern in Fig. 6b shrinks (more obviously at the low V_G end) without the extrinsic charge model, indicating that the capacitance sensitivity to bias is lower. This is because only the intrinsic capacitance is activated, which contributes insufficient bias-dependent capacitance without extrinsic capacitance modeled by the PSP extrinsic charge model.

S-parameters of the cross-coupled NMOS is measured at the zero-biased condition, then converted into Y-parameter and de-embedded with Y-parameters of the open GSG PAD structure. These de-embedded Y-parameters include the admittance introduced by NMOS, which need to be subtracted before extracting interconnection parasitic admittance, $Y_{\text{interconnect}}$ in Eqs. (11) and (12). After subtracting the NMOS-introduced admittance, these Y-parameters are converted to three separated sets of admittance curves, Y_P, Y_N, and Y_X, with Eqs. (11) and (12) for extracting parasitics of the interconnection using vector fitting. The extracted values of the parameters in Fig. 5 are listed in Table 2, and the fitting results are shown in Fig. 7. Although there are negative R/L/C values, the lumped network is stable and works well with the MOS model without the convergence problem.

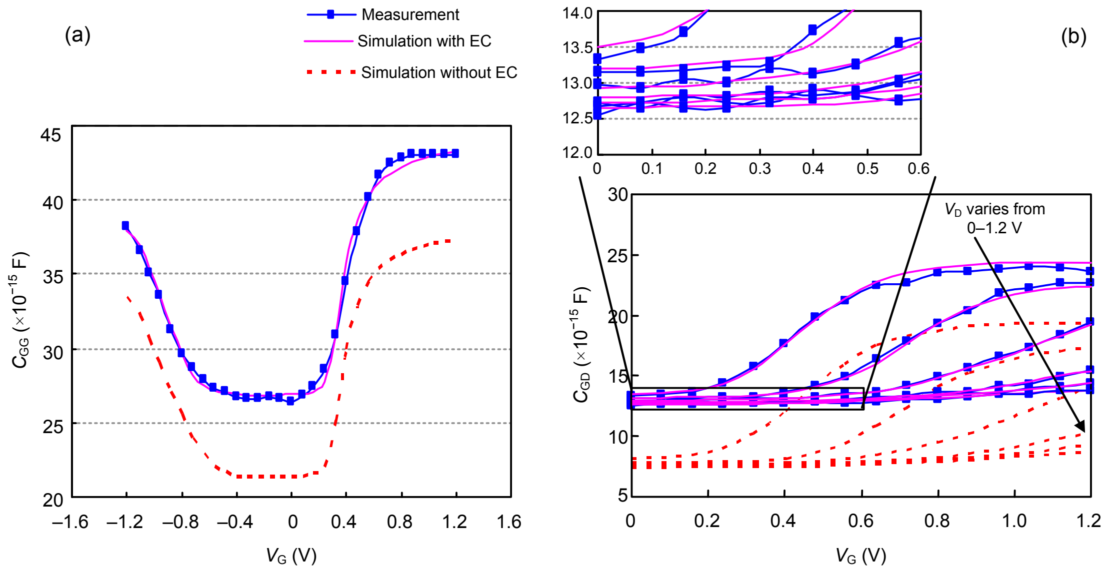

Fig. 6 Fitting results of MOS capacitance at 1 GHz after PSP charge model parameters are extracted, compared with simulation without the PSP extrinsic charge (EC) model: (a) $C_{GG}(V_G)$; (b) $C_{GD}(V_G, V_D)$

Table 2 Resistor/inductor/capacitor parameters extracted by vector fitting

	Parameter	Value
Y_P or Y_N	R_T (Ω)	45.251
	R_{TA1} (Ω)	−53.77
	R_{TA2} (Ω)	−285.76
	R_{TA3} (Ω)	142 710
	R_{TA4} (Ω)	−118 880
	C_T (F)	30.71×10^{-15}
	L_{TA1} (H)	-35.666×10^{-15}
	L_{TA2} (H)	-669.68×10^{-15}
	L_{TA3} (H)	50.502×10^{-6}
	L_{TA4} (H)	-102.71×10^{-6}
Y_X	R_X (Ω)	8.546
	R_{XA1} (Ω)	−8.453
	R_{XA2} (Ω)	775.51
	R_{XA3} (Ω)	−426 570
	R_{XA4} (Ω)	428 640
	C_X (F)	-23.758×10^{-15}
	L_{XA1} (H)	-2.041×10^{-12}
	L_{XA2} (H)	1.832×10^{-9}
	L_{XA3} (H)	-45.418×10^{-6}
	L_{XA4} (H)	608.09×10^{-6}

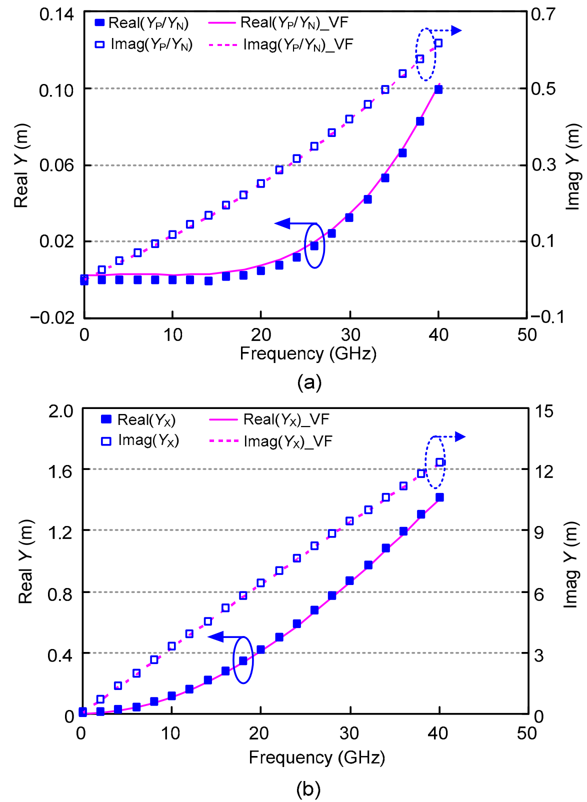

Fig. 7 Fitting results of the interconnect parasitics by vector fitting (VF) up to 40 GHz: (a) Y_P or Y_N; (b) Y_X

An NMOS-only LC VCO adopting a bonding wire inductor is fabricated to validate the model (Fig. 8). Fundamental outputs of the VCO are eliminated to avoid the extra bias-dependent capacitance introduced by the buffer. Oscillation signal is exported from the second harmonic node to alleviate the capacitance load introduced by the printed circuit board (PCB) test board. The bonding wire inductance is extracted in a high frequency structure simulator (HFSS). Simulation efficiency and convergence for both the process design kit (PDK) reference (BSIM3v3 intrinsic core with a numerical-function-based extrinsic gate capacitance model) and the proposed model (PSP 102.3 intrinsic core with the PSP charge model for the extrinsic gate capacitance) are evaluated with the pre-layout PSS simulation, which excludes the interconnection parasitics. Besides, the same junction capacitance model is used for both the reference and the proposed models. Simulation time at different V_{DD}, which is the mean value of 10 simulations, and the average simulation time totally consumed at different V_{DD} are shown in Fig. 9. The reference model suffers from a convergence problem when V_{DD} equals 0.7 or 0.8 V. Discarding the non-convergence situations, the average simulation times at different V_{DD} are 1.612 and 0.636 s for the reference and the proposed models, respectively, with the efficiency enhancement up to 60.5%.

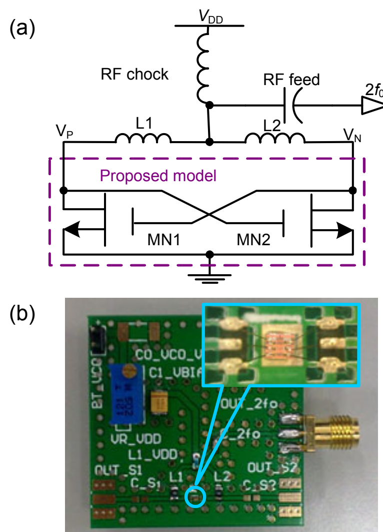

Fig. 8 Schematic of the NMOS-only voltage controlled oscillator (VCO) where signal is exported from the 2nd harmonic node while V_{DD} is used to tune the output frequency (a) and the test board for the VCO (b)

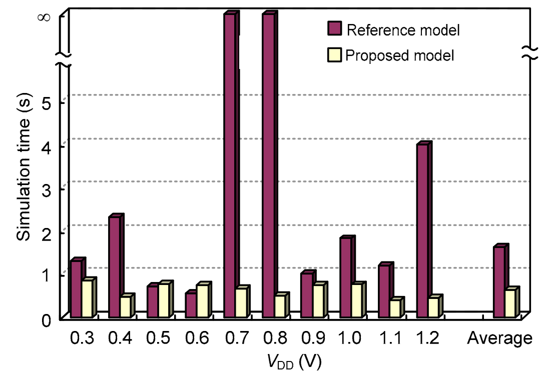

Fig. 9 Comparison of the simulation time between the reference PDK model and the proposed model in the pre-layout periodic-stead-state (PSS) simulation

Simulation time of the reference model approaches infinity at V_{DD}=0.7 or 0.8 V. This means the reference model suffers from the convergence problem, and the values at these points are discarded when calculating the average time. Simulation runs on a workstation of Xeon 1.86 GHz CPU and 2 GB RAM, with MMSIM710

Fig. 10 shows the VCO frequency characteristics versus tuning V_{DD} obtained from the post-layout simulation by the PDK reference model and the proposed model, and from measurement. Given the large number of post-layout parasitic capacitances and the poor convergence, the PSS simulation by the reference model is extremely slow and frequently turns to errors. Therefore, the transient simulation is adopted to calculate the oscillating frequency for the reference model instead of the PSS simulation. Results show that the proposed model is more accurate, and the relative RMS errors are 0.934% and 0.357% for the reference and proposed models, respectively, with the accuracy enhancement up to 61.8%. Moreover, the reference model performs well only at the intermediate supply region between 0.6–0.9 V. The extrinsic gate capacitance is underestimated at the higher region, while it is overestimated at the lower region by numerical functions. For further insights, this VCO operates in the voltage-limited region; and when VCO is biased in the intermediate supply region, NMOS works linearly most of the time within an oscillation period, and the numerical function (Eq. (7)) fitted with S-parameters characterizes the extrinsic gate capacitance well except for the convergence problem. However, as the bias goes higher or lower, non-linearity of NMOS becomes more significant, and the numerical function fails to accurately

characterize the extrinsic capacitance even though it is fitted quite well by *S*-parameters. This phenomenon proves that the numerical model which is well-fitted by *S*-parameters does not guarantee accuracy of non-linear simulations as mentioned above, and for this reason, a physical-based model for extrinsic gate capacitance is crucial.

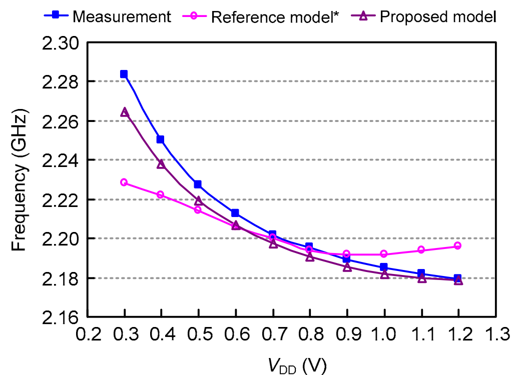

Fig. 10 Frequency tuning characteristics of the VCO design obtained from post-layout simulation by the reference and the proposed models as well as from measurement

* Considering the inefficiency and poor convergence of the reference model, the oscillating frequency is derived from the transient simulation instead of PSS simulation

5 Conclusions

An efficient model for layout-optimized cross-coupled MOSFETs in VCO is presented. This model considers the cross-coupled MOSFETs as a unit device. In this model, the PSP charge model is adopted to characterize the bias-dependent capacitance instead of normally-used numerical functions of strong non-linearity, which improves the simulation convergence. An original scheme for extracting PSP charge model parameters is developed based on *S*-parameters measurement. Vector fitting is utilized to model the interconnections, which is more accurate and efficient in circuit-level simulation in comparison with post-layout parasitics extraction. An NMOS-only LC VCO is designed and fabricated to verify this model. Experimental results show that the proposed model has no convergence problem and achieves improvements up to 60.5% and 61.8% in simulation efficiency and accuracy, respectively. This model is applicable to the optimized cross-coupled MOSFETs in advanced RF circuit design.

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